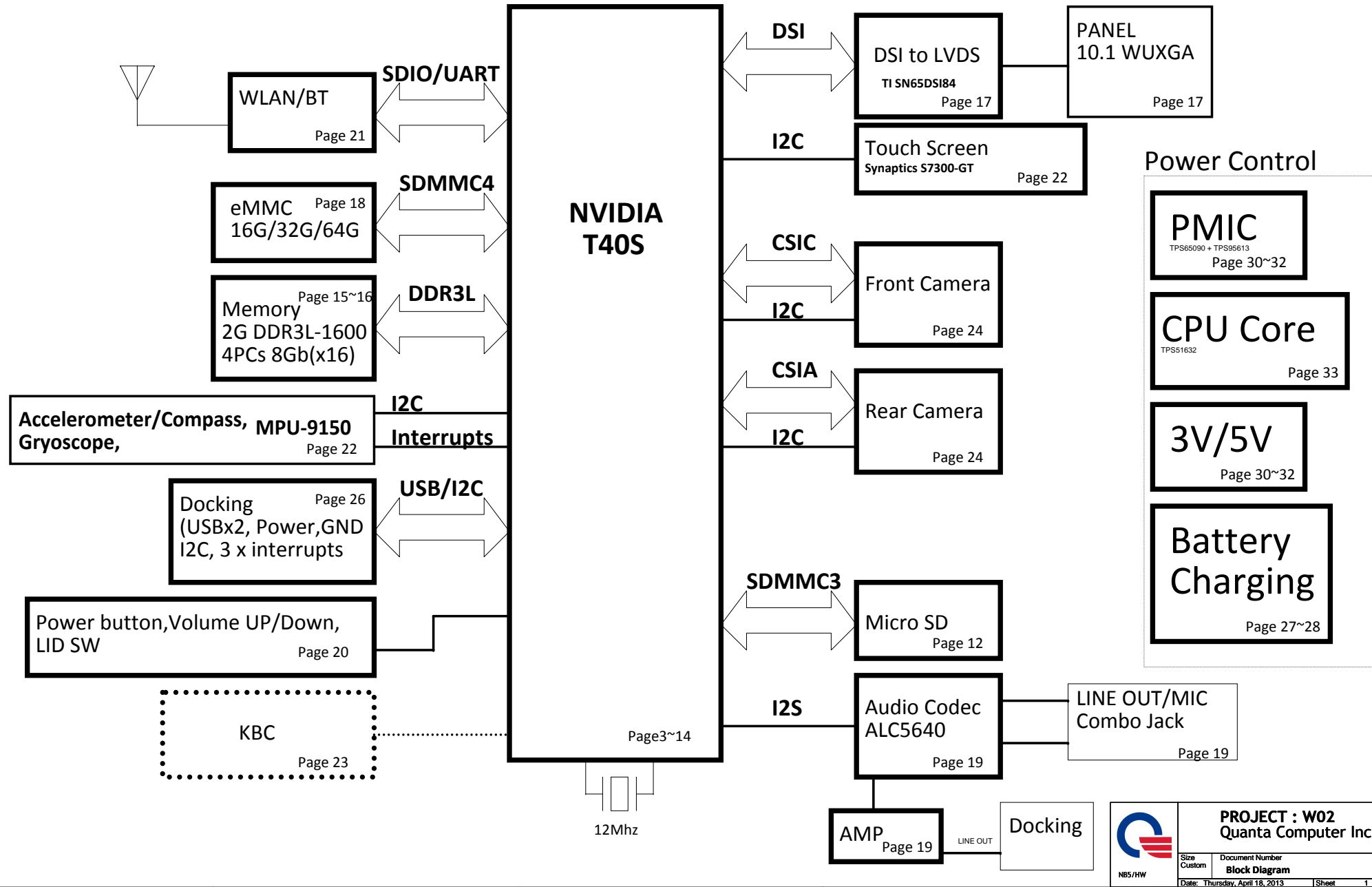
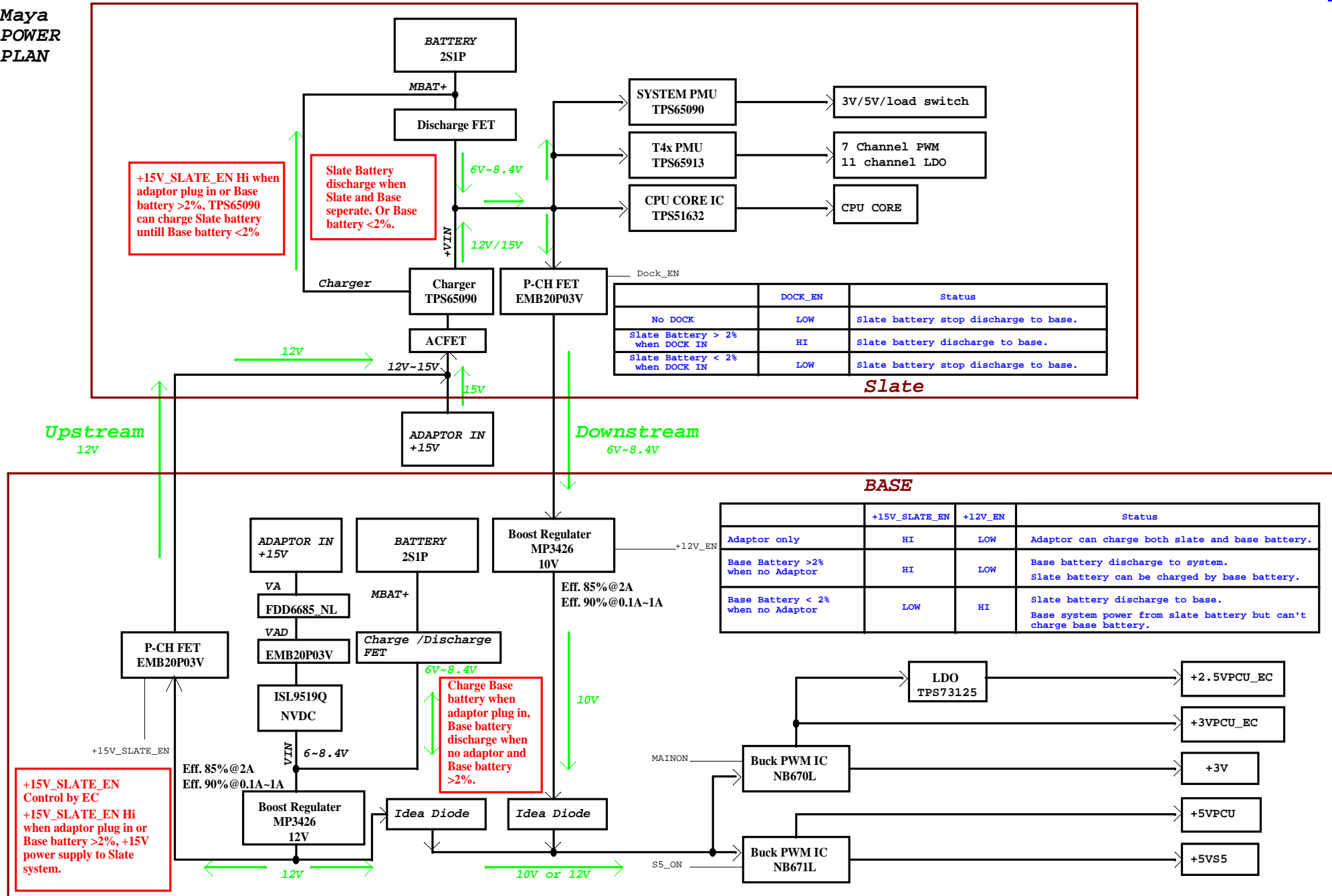
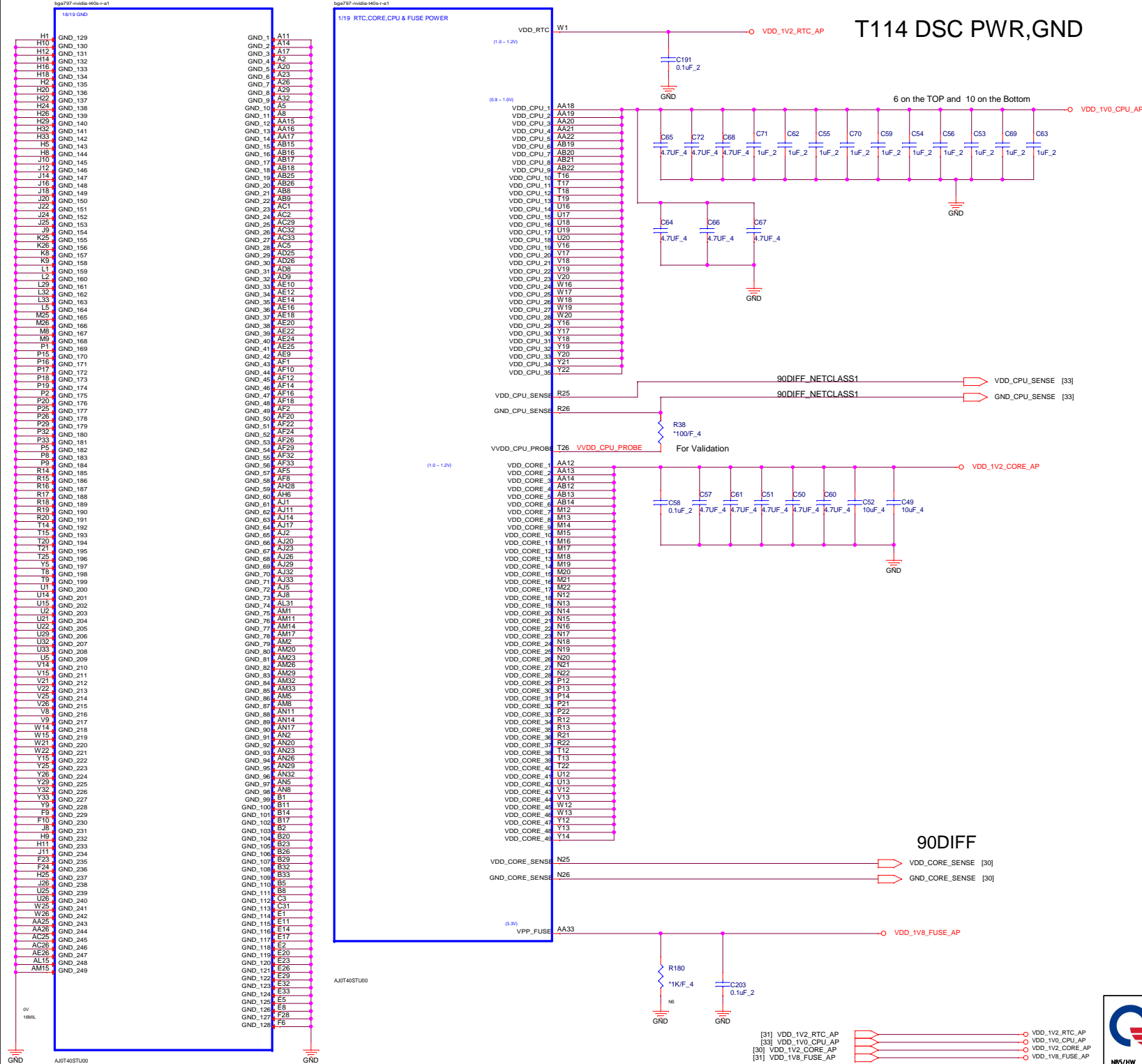


Maya W02 Tegra4 (T40S) Platform Block Diagram



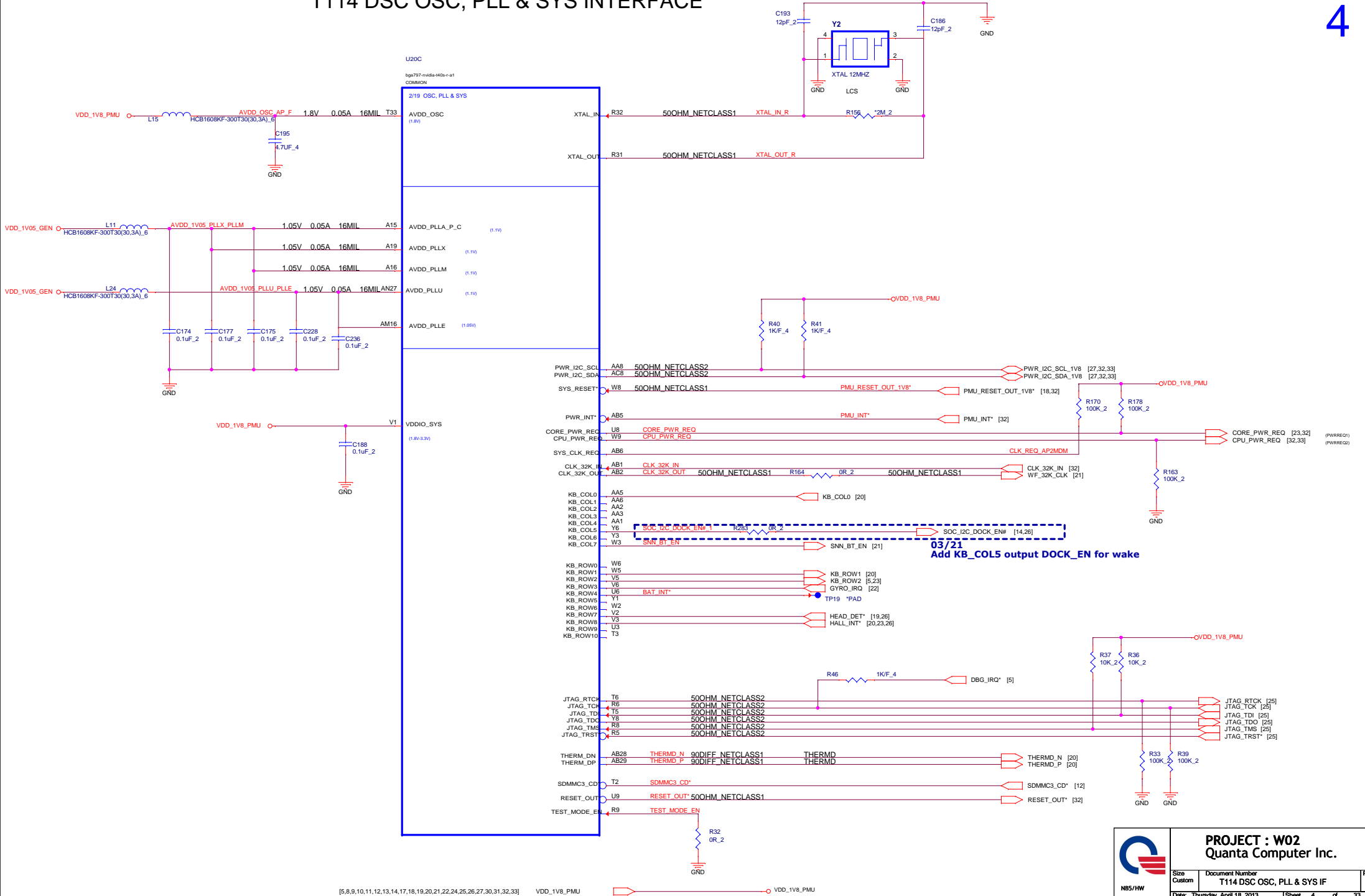
Maya POWER PLAN

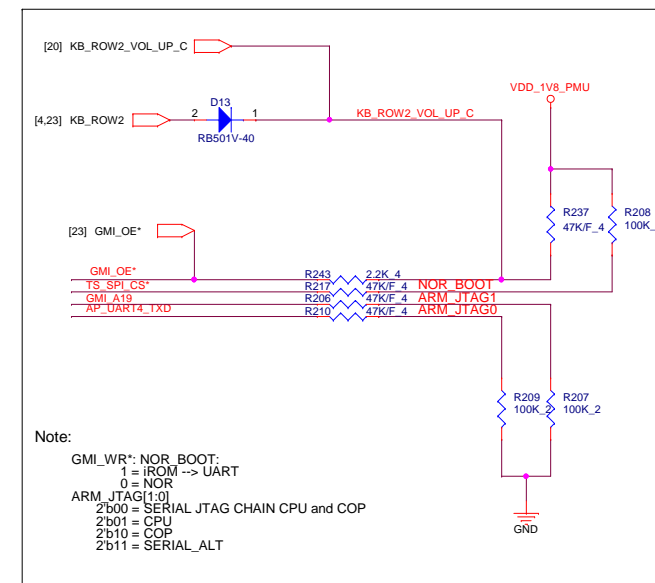
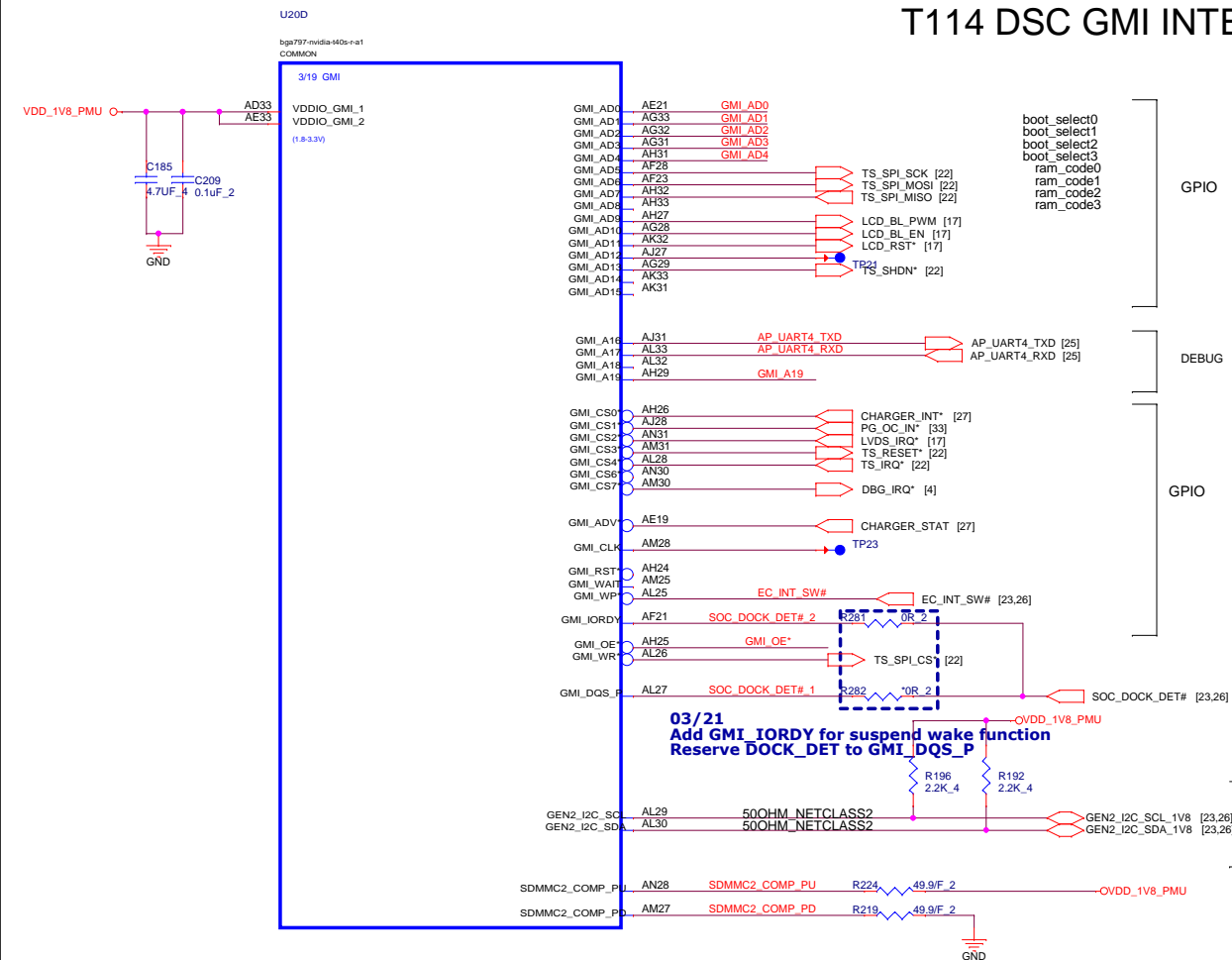




T114 DSC OSC, PLL & SYS INTERFACE

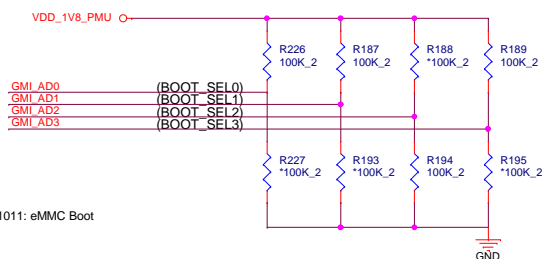
4



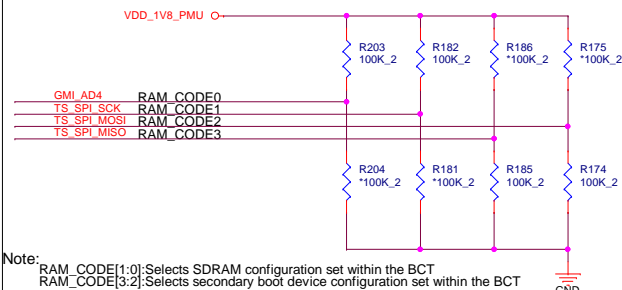


DDR3L				
TOPBSQ	QBCON	QCI PN	Vender PN	Description
		AKD5JGETW00	H5TC4G63AFR-PBA	IC SDRAM(96P)H5TC4G63AFR-PBA(FBGA) Hynix (default)
		AKD5JGST403	EDJ4216EFBG-GN-F	IC SDRAM (96P) EDJ4216EFBG-GN-F(FBGA) Elpida
		AKD5JGSTL02	MT41K256M16HA-125-E	IC SDRAM(96P) MT41K256M16HA-125-E (FBGA) Micron

Boot Source: eMMC as default



RAM code



Memory Strap pin :

Hynix : (default)
Hynix : H5TC4G63AFR-PBA
RAM_CODE0 : 1
RAM_CODE1 : 1
Micron :
Micron : MT41K256M16HA-125:E
RAM_CODE0 : 1
RAM_CODE1 : 0
Elpida :
Elpida : EDJ4216EFBG-GN-F
RAM_CODE0 : 0
RAM_CODE1 : 1



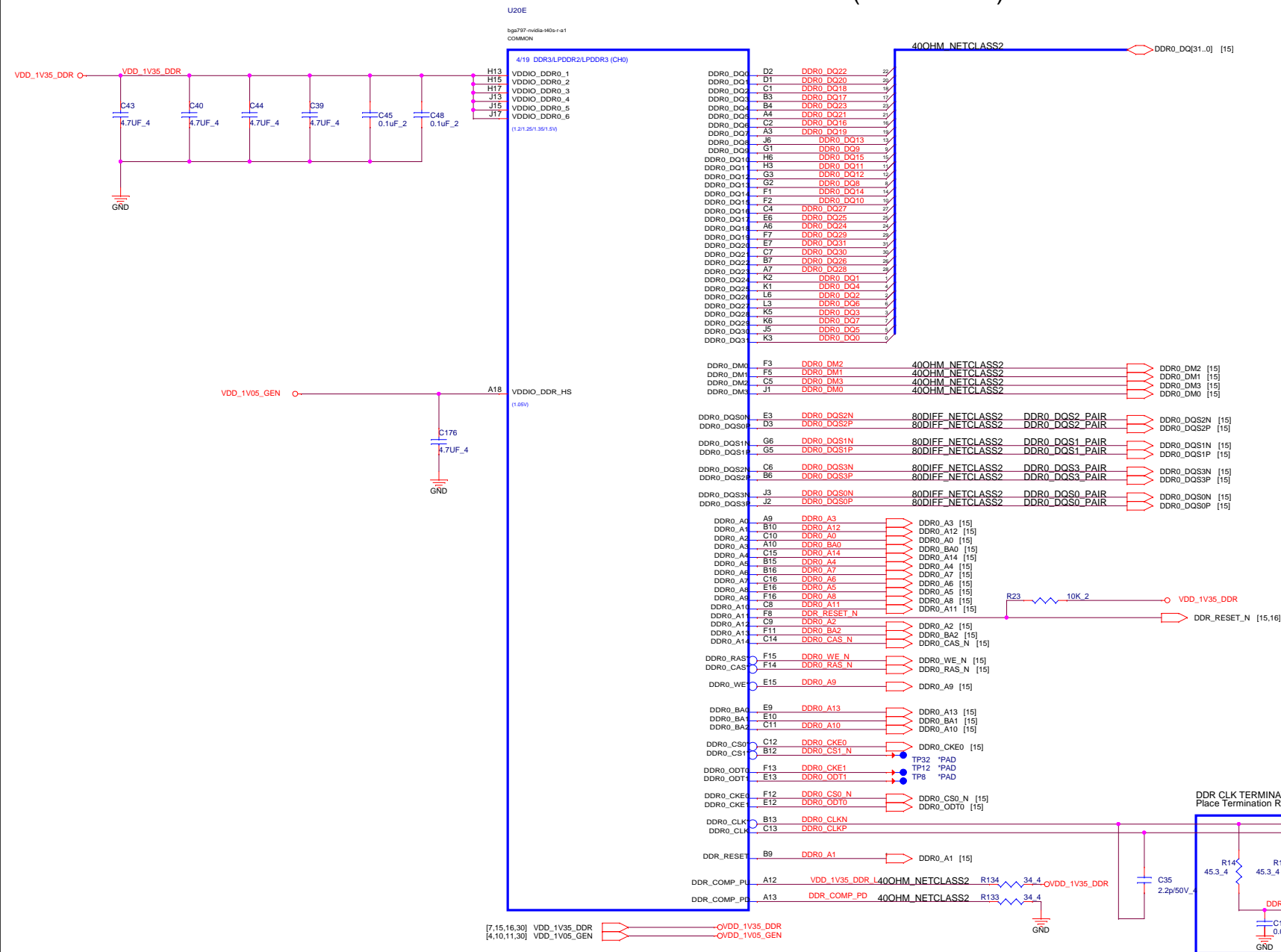
PROJECT : W02
Quanta Computer Inc.

Size	Document Number	Rev
Custom	T114 DSC GMI & BOOT STRAP	1A
Date: Thursday, April 18, 2013	Sheet 5 of 33	

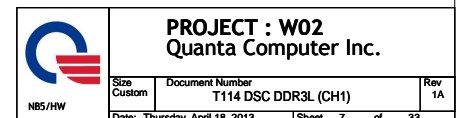
[4,8,9,10,11,12,13,14,17,18,19,20,21,22,24,25,26,27,30,31,32,33] VDD_1V8_PMU

T114 DSC DDR3L INTERFACE (CHANNEL0)

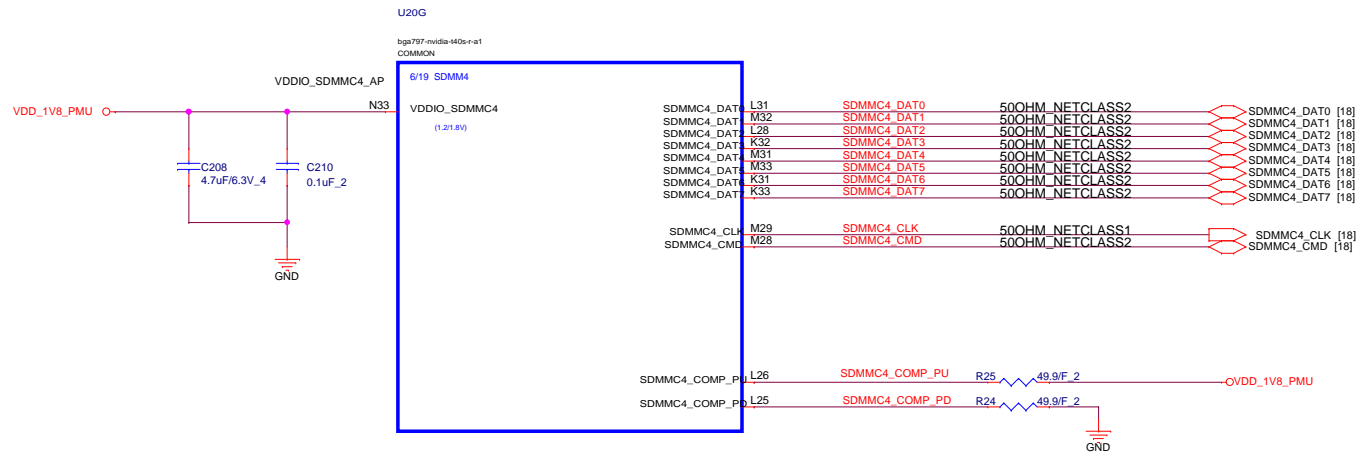
6



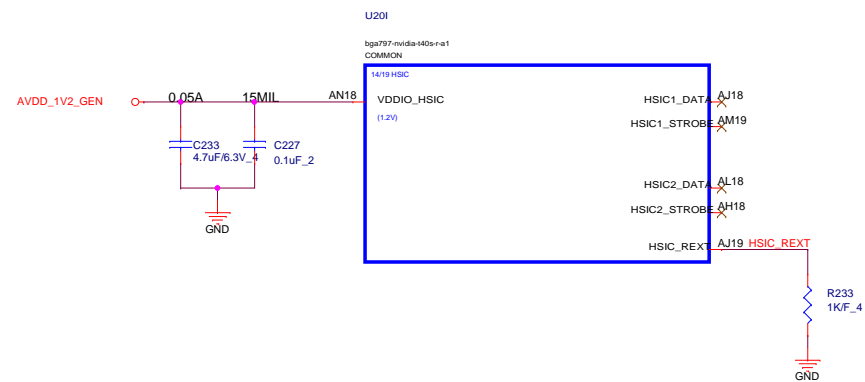
7



T114 DSC SDMMC4 INTERFACE

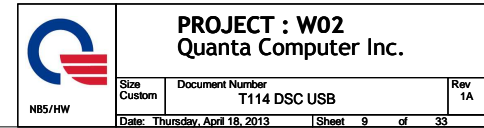


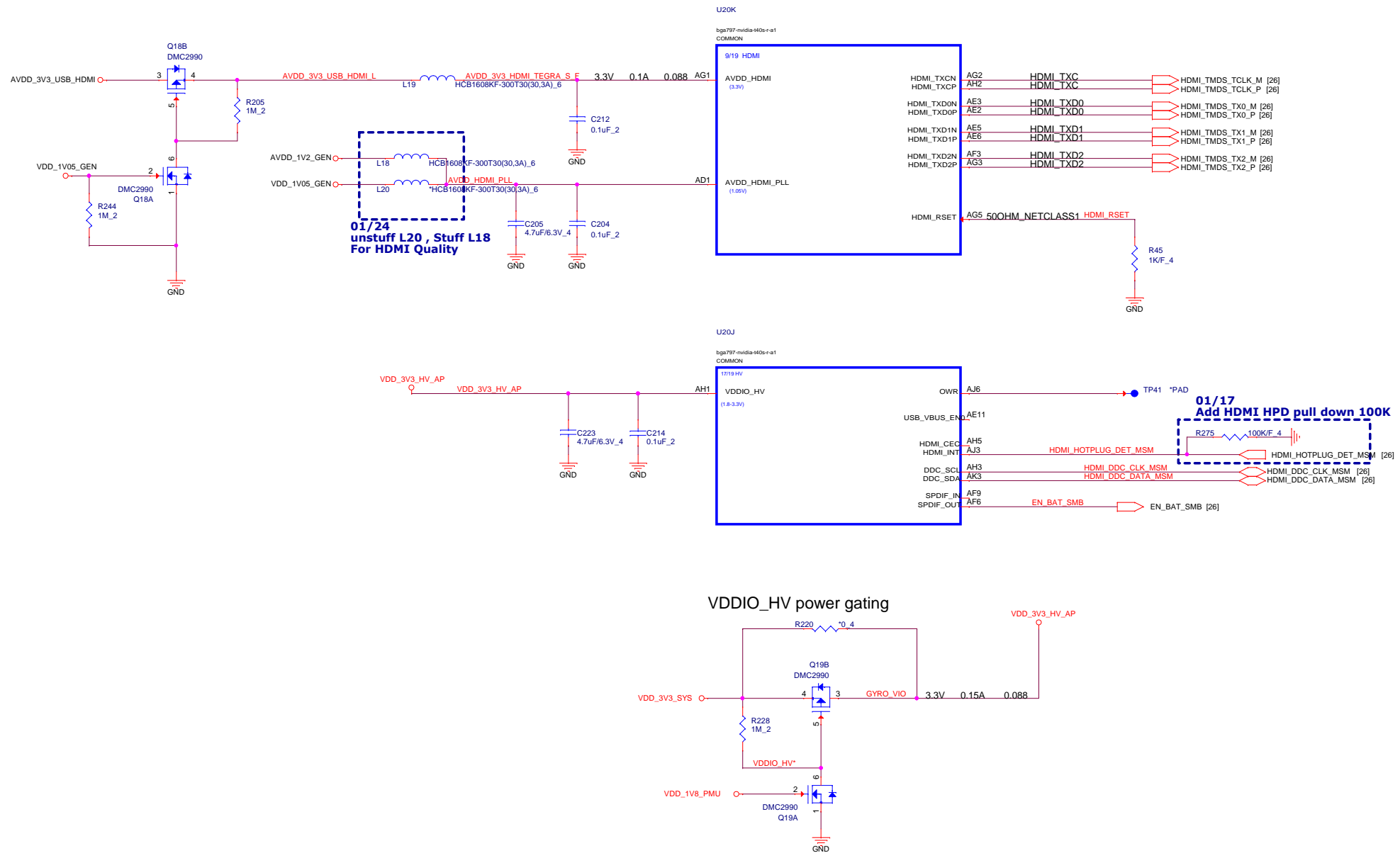
T114 DSC HIGH SPEED INTERCHIP



[10,11,31] AVDD_1V2_GEN AVDD_1V2_GEN
[4,5,9,10,11,12,13,14,17,18,19,20,21,22,24,25,26,27,30,31,32,33] VDD_1V8_PMU VDD_1V8_PMU

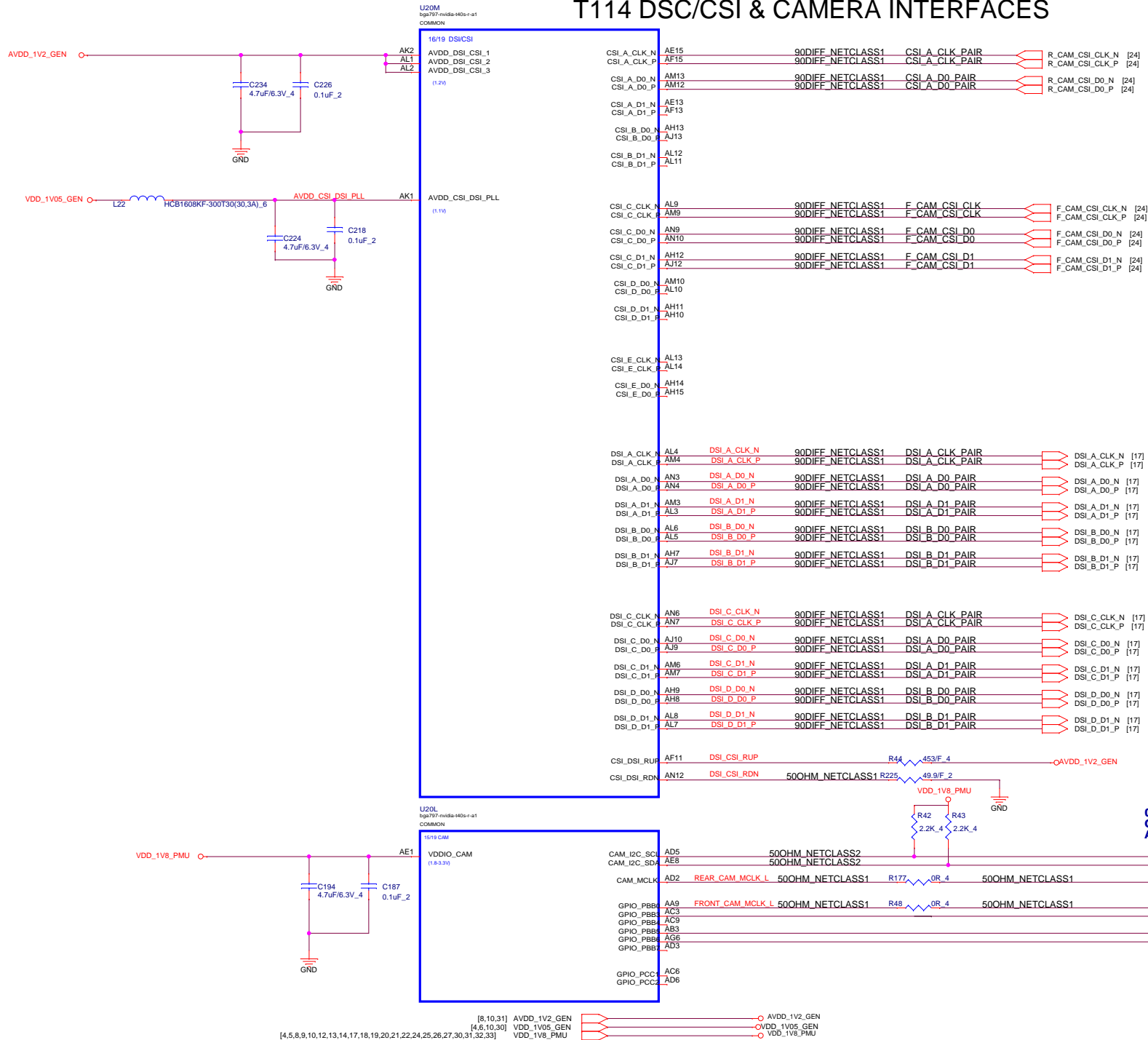
9





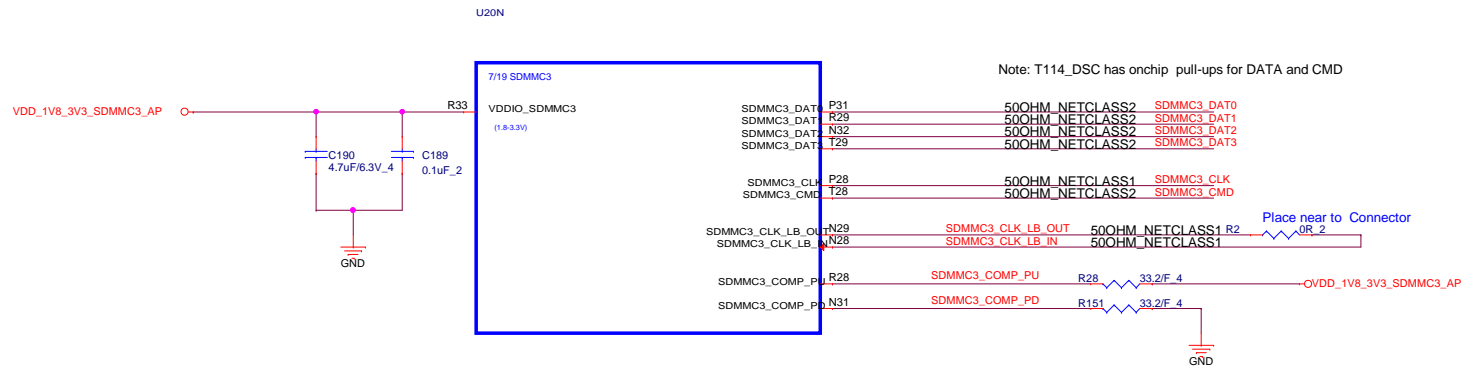
[9,31] AVDD_3V3_USB_HDMI
[4,6,11,30] VDD_1V05_GEN

T114 DSC/CSI & CAMERA INTERFACES



PROJECT : W02
Quanta Computer Inc.

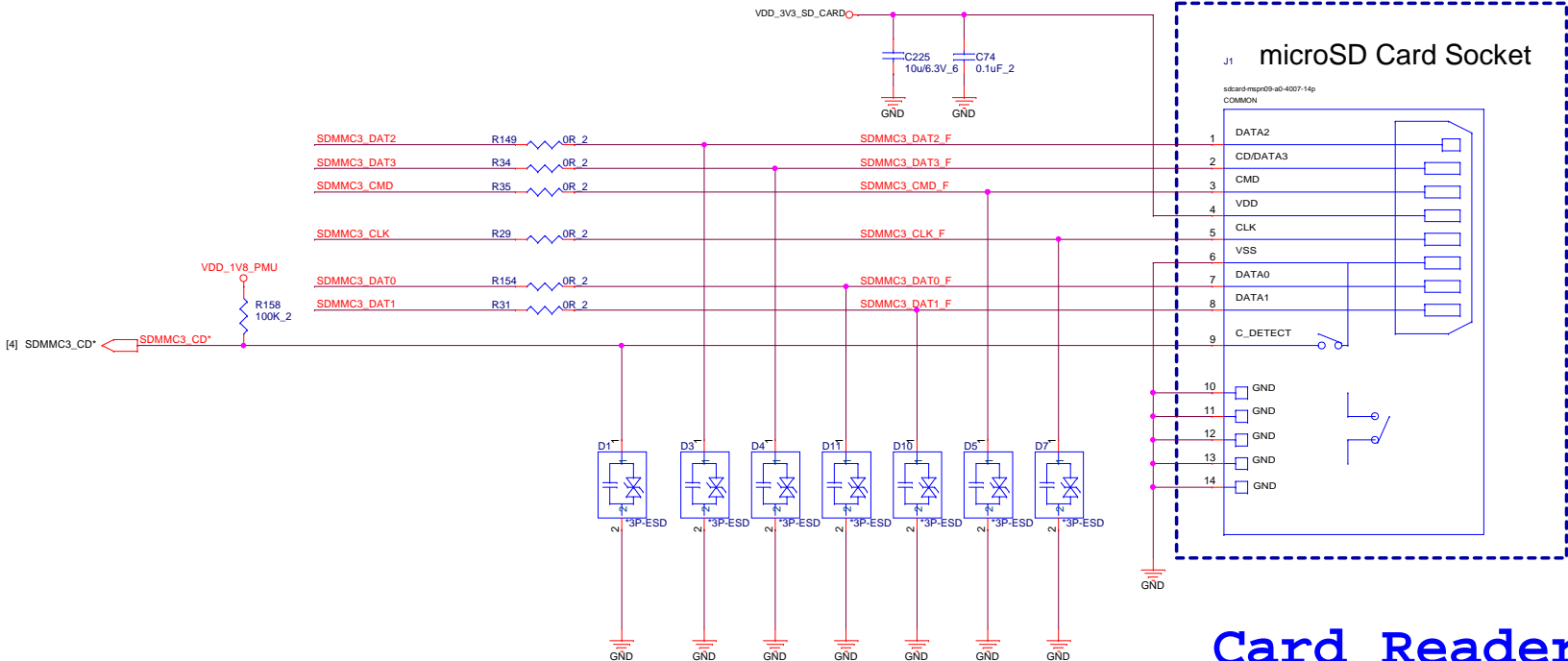
Size Custom	Document Number T114 DSC/CSI & CAMERA	Rev 1A
Date: Thursday, April 18, 2013	Sheet 11 of 33	



Place close to J1

確認 footprint

01/07
Swap Pin9 . 12
Correct pin define



Card Reader

Note: Place those diodes close to the SD socket

[31] VDD_1V8_3V3_SDMMC3_AP

[29] VDD_3V3_SD_CARD

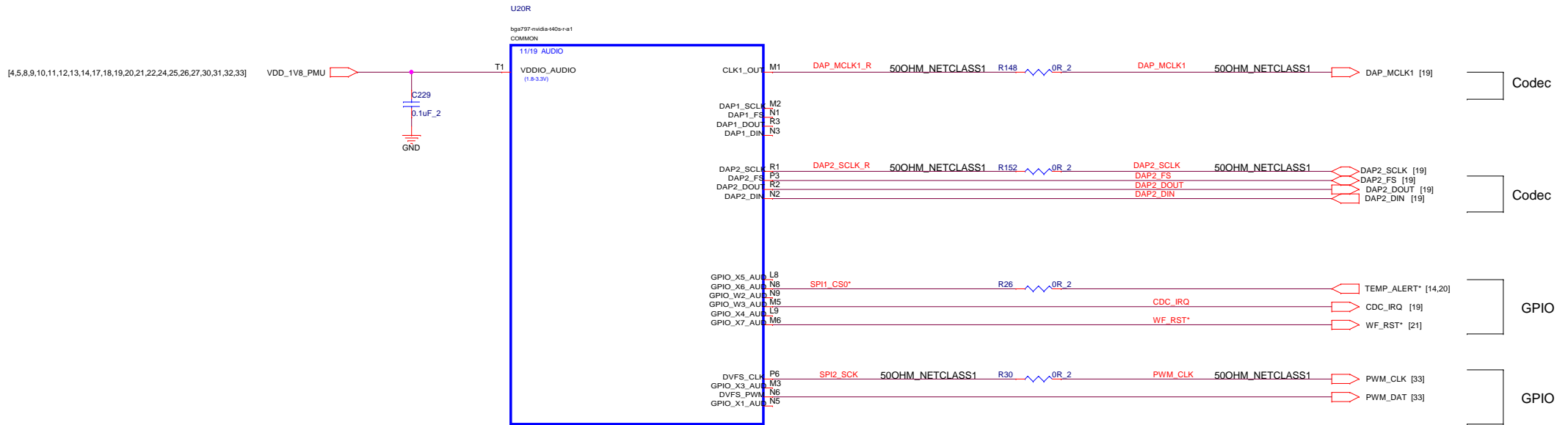


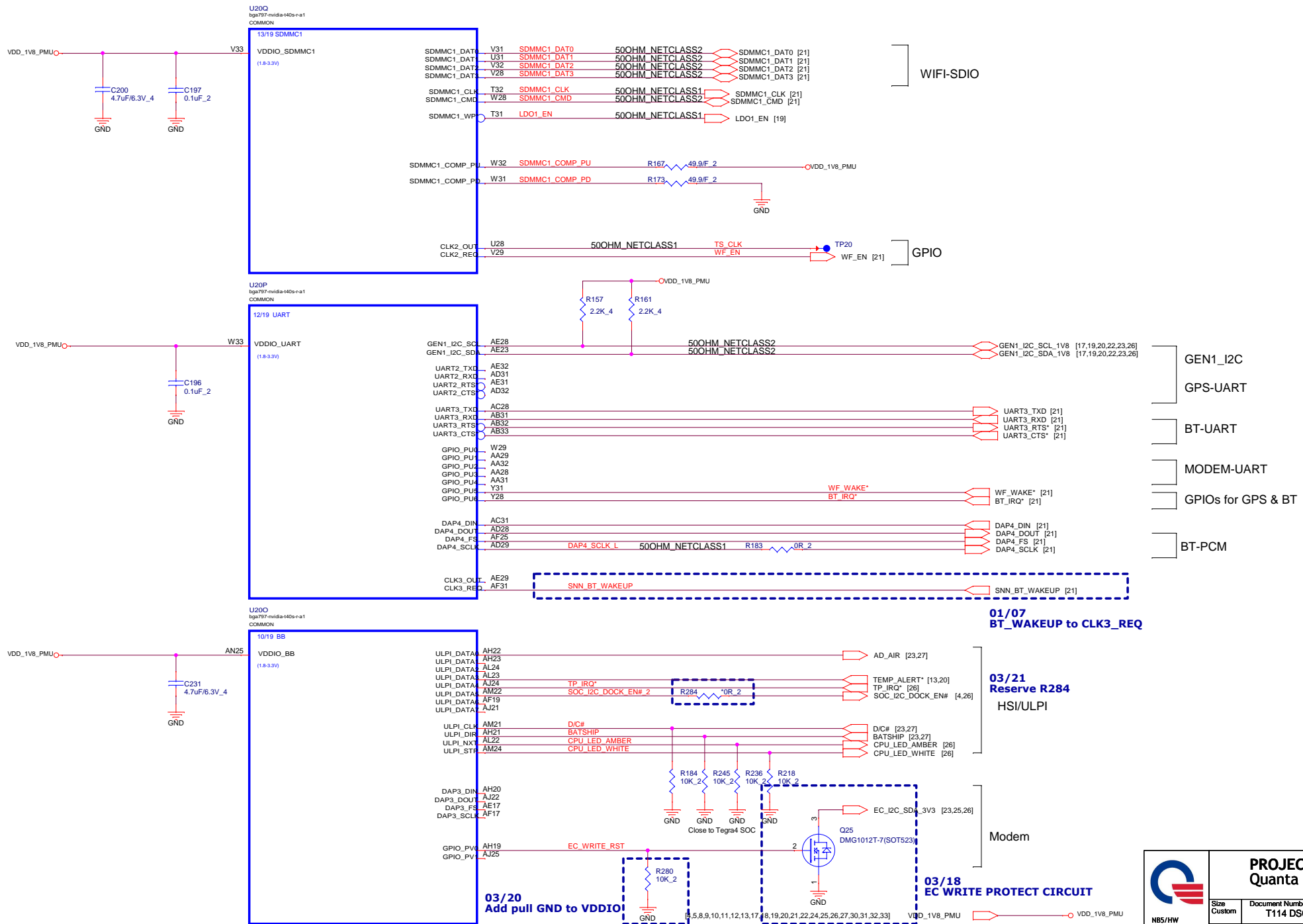
PROJECT : W02
Quanta Computer Inc.

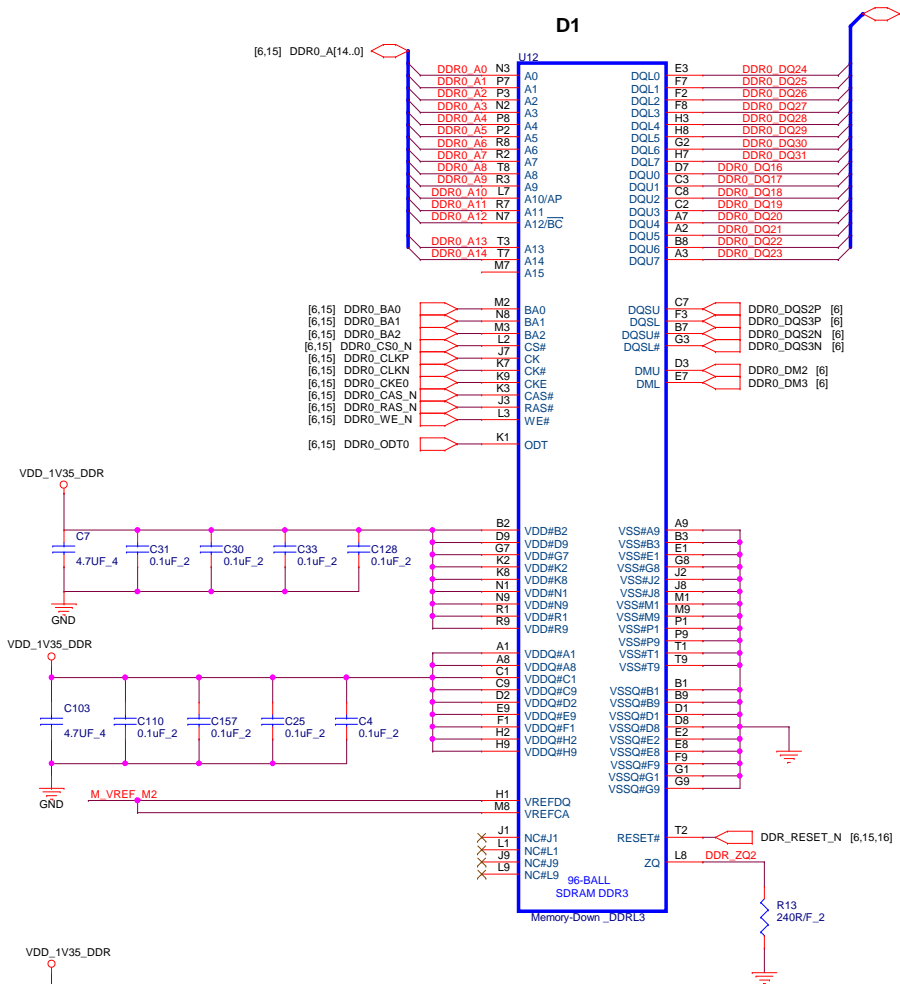
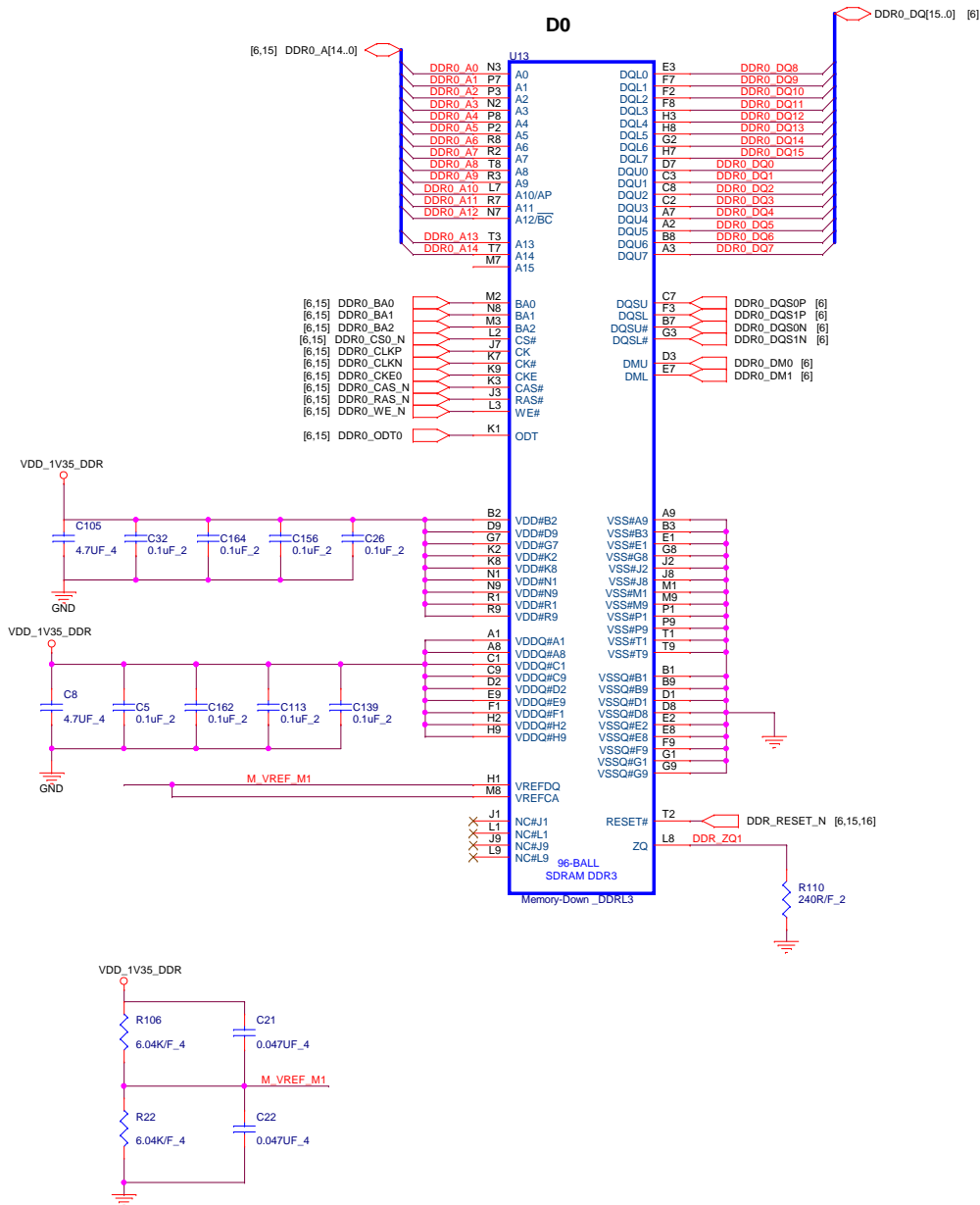
Size Custom	Document Number T114 DSC SDMMC3 & SD Card	Rev 1A
Date: Thursday, April 18, 2013	Sheet 12 of 33	

T114 DSC AUDIO INTERFACE

13







DDR3L			
QCI PN	Vender PN	Description	
AKD5JGETW00	HSTC4G63AFR-PBA	IC SDRAM(96P)H5TC4G63AFR-PBA(FBGA)	Hynix (default)
AKD5JGST403	EDJ4216EFBG-GN-F	IC SDRAM (96P) EDJ4216EFBG-GN-F(FBGA)	Elpida



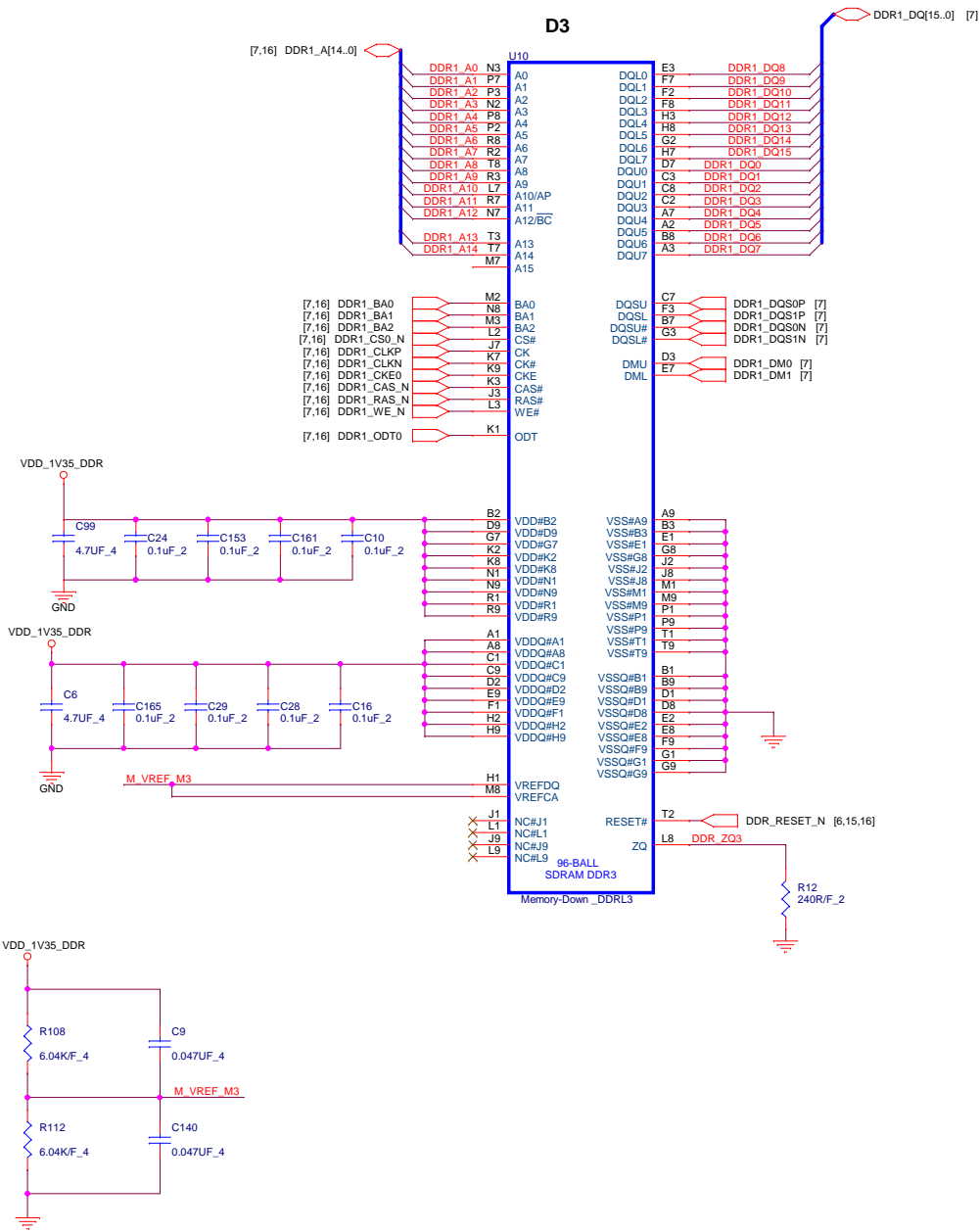
PROJECT : W02
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (A) On Board_A,1Rank	1A
Date: Thursday, April 18, 2013	Sheet 15 of 33	

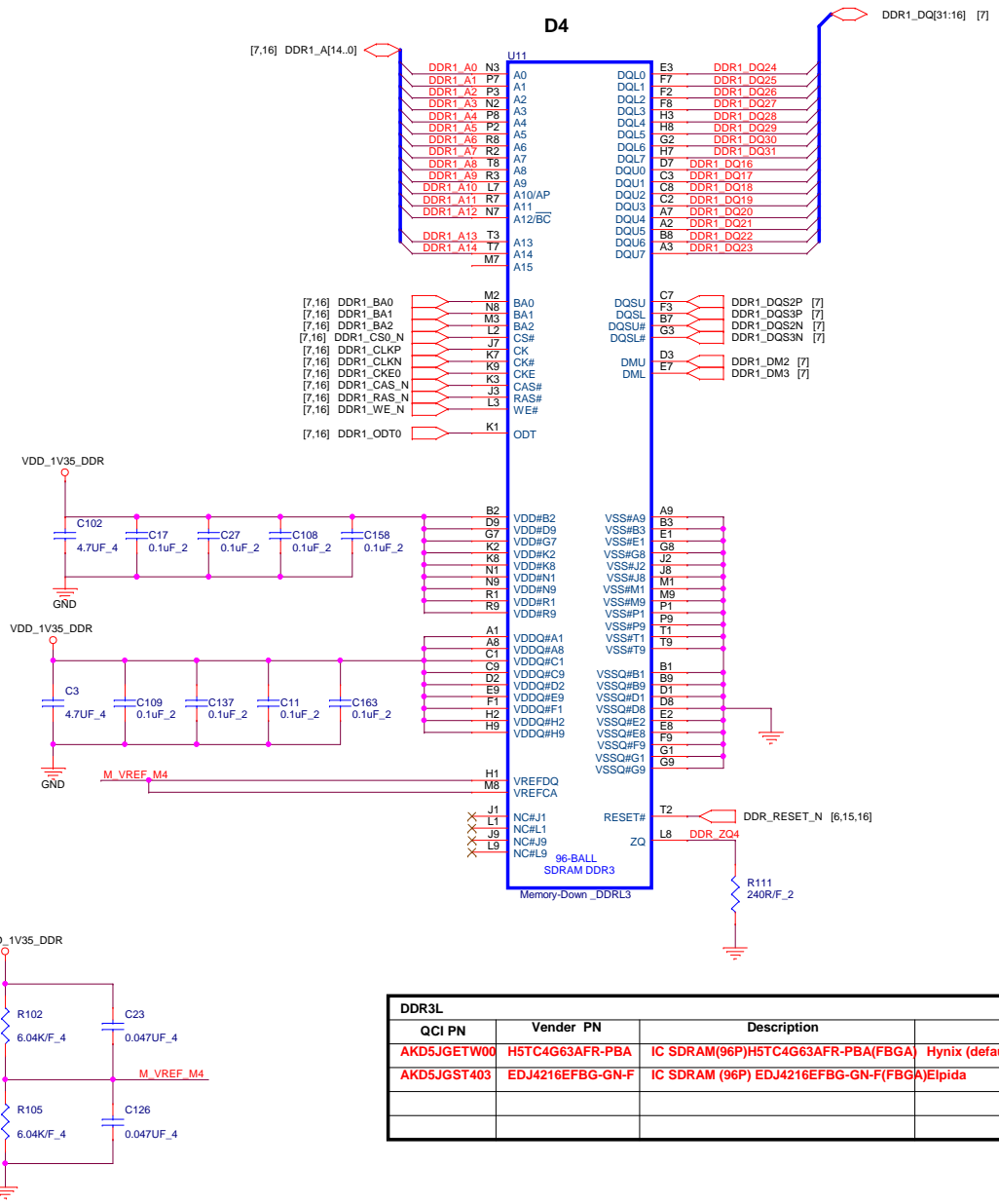
[6,7,16,30] VDD_1V35_DDR

OVDD_1V35_DDR

D3



D4



QCI PN	Vender PN	Description	
AKD5JGETW00	HSTC4G63AFR-PBA	IC SDRAM(96P)HSTC4G63AFR-PBA(FBGA)	Hynix (default)
AKD5JGST403	EDJ4216EFBG-GN-F	IC SDRAM (96P) EDJ4216EFBG-GN-F(FBGA)	Elpida

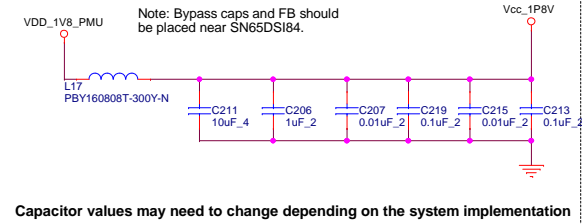


PROJECT : W02
Quantia Computer Inc.

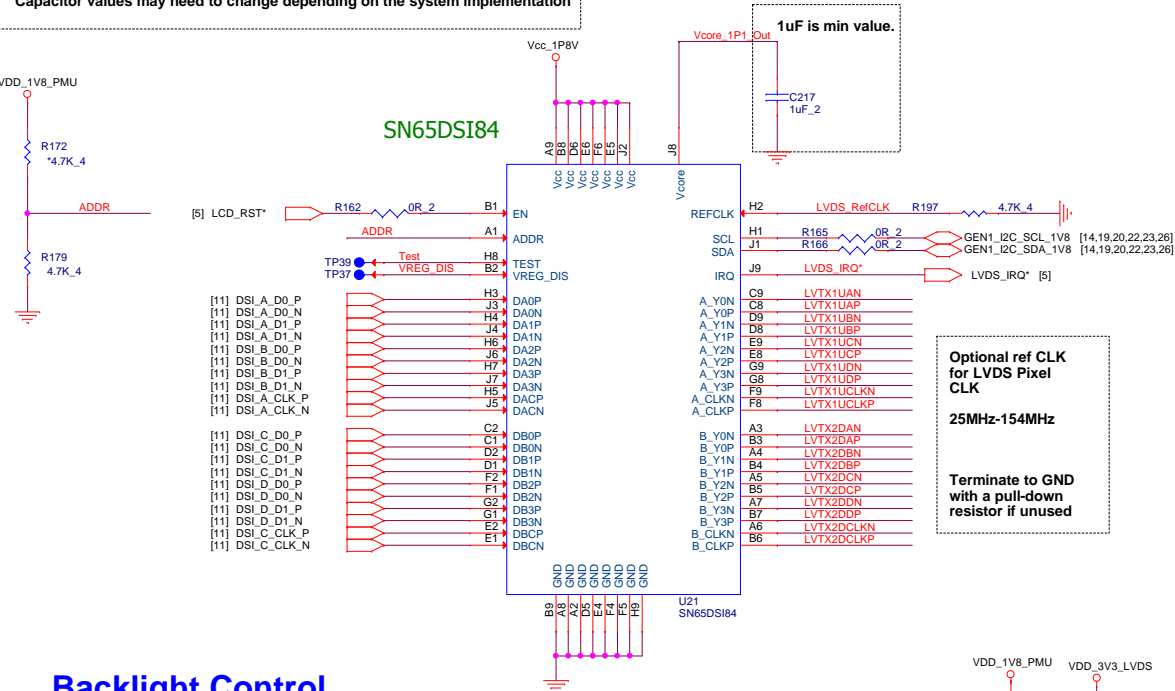
Size	Document Number	Rev
	DDR3 (A) On Board_A,2Rank	
Date: Thursday, April 18, 2013	Sheet	16 of 33

[6,7,15,30] VDD_1V35_DDR VDD_1V35_DDR

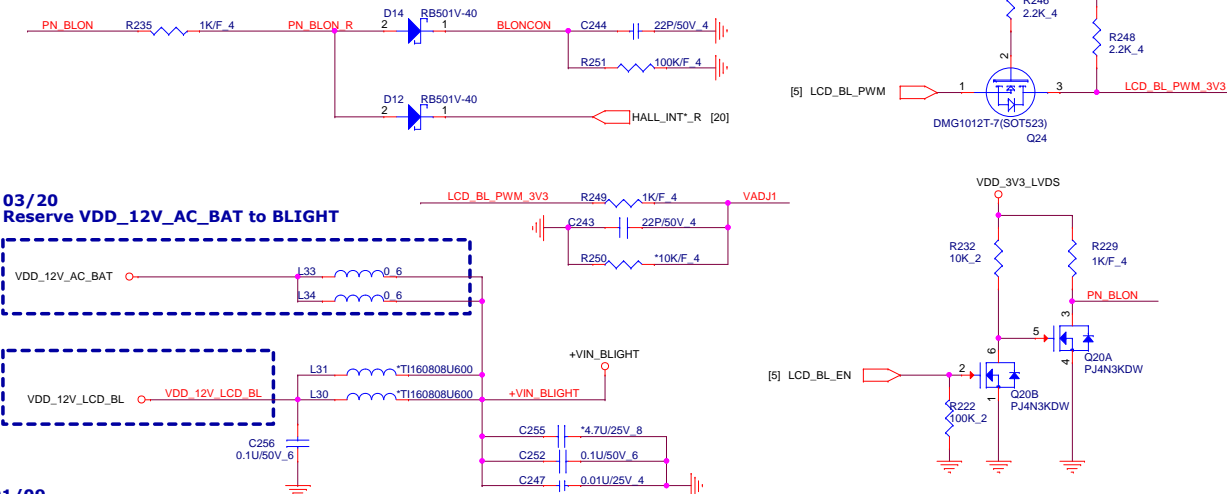
DSI to LVDS Bridge



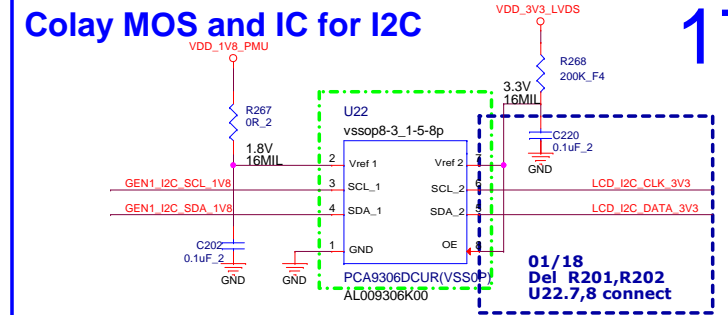
SN65DSI84



Backlight Control

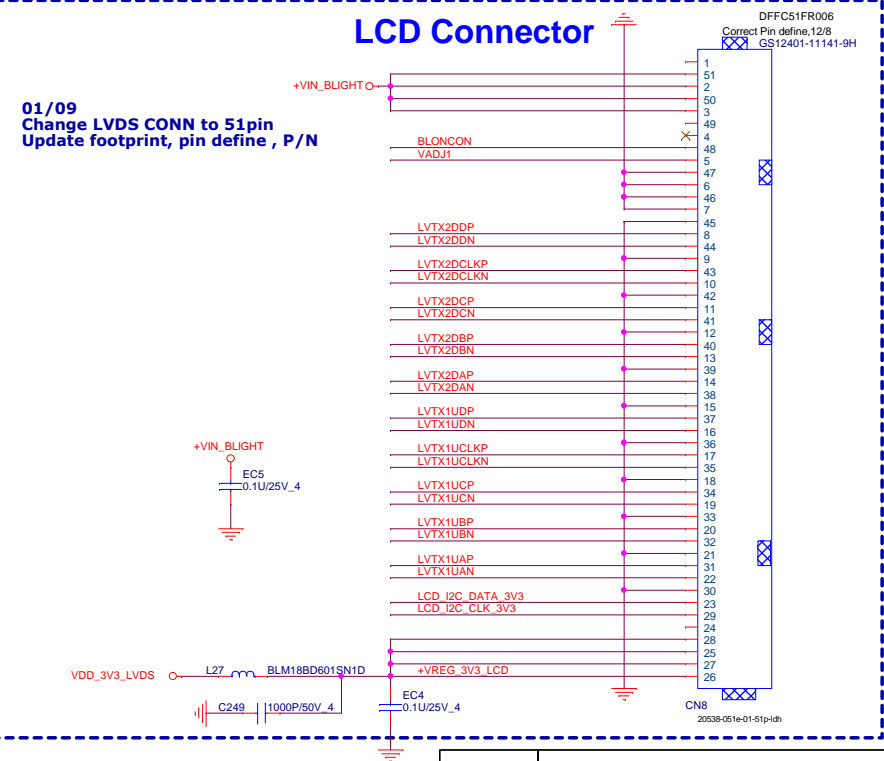


Colay MOS and IC for I2C



LCD Connector

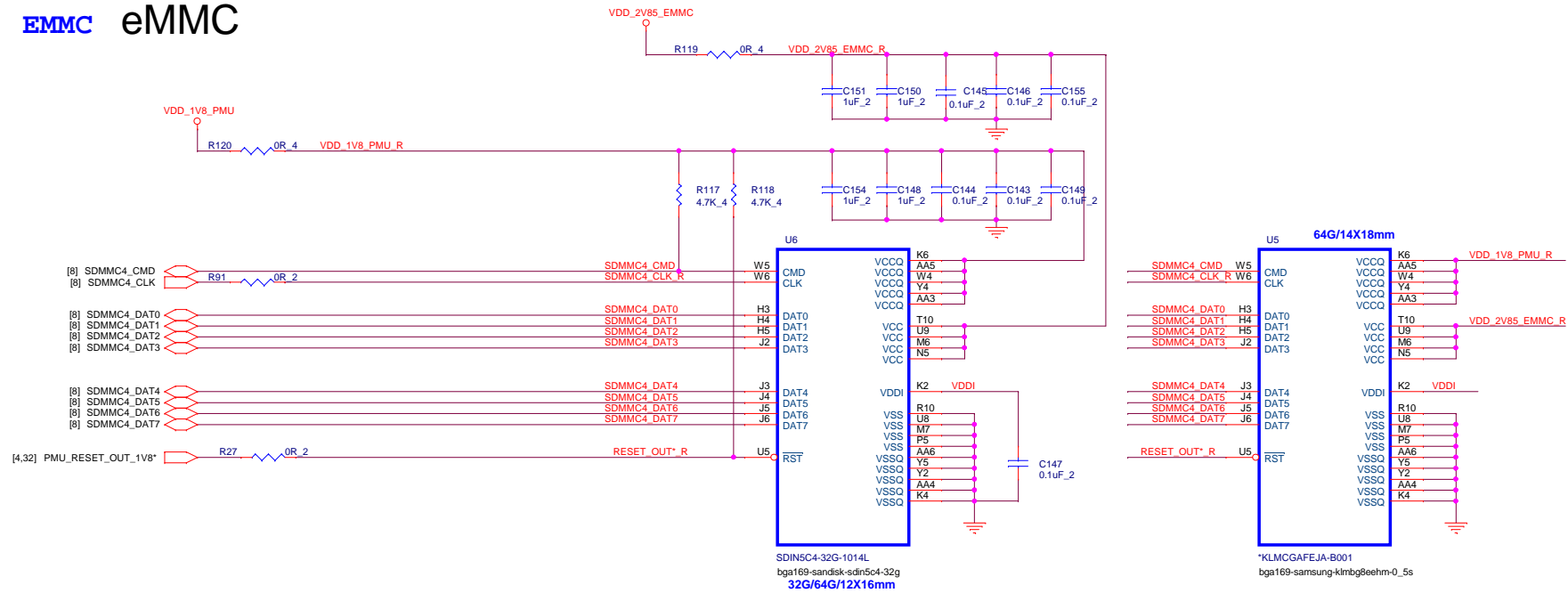
01/09 Change LVDS CONN to 51pin
Update footprint, pin define , P / N



PROJECT : W02
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISPLAY CONNECTOR	1A
Date: Thursday, April 18, 2013	Sheet 17 of 33	

EMMC eMMC



iNAND (eMMC)				
TOPBSQ	QBCON	Description	SIZE	
AKE3RZPT101	AKE3RZPT102	IC FLASH(169P) SDIN5C4-16G-1014L TOP BSQ	16G/*X*mm	Sandisk
AKE3SZPT102	AKE3SZPT101	IC FLASH(169P)SDIN5C4-32G-1014L TOPBSQ	32G/*X*mm	Sandisk
AKE3TZPT101	AKE3TZPT100	IC FLASH(169P)SDIN5C4-64G-1014L TOPBSQ	64G/*X*mm	Sandisk
AKE3RYPT503	AKE3RYPT504	IC FLASH(169P) KLMBG2GE4A-A001 TOP BSQ	16G/*X*mm	Samsung
AKE3SZPT504	AKE3SZPT503	IC FLASH(169P)KLMBG4GE4A-A001 TOPBSQ	32G/*X*mm	Samsung
AKE3TZPT504	AKE3TZPT503	IC FLASH(169P)KLMBG8GE4A-A001 TOPBSQ	64G/*X*mm	Samsung

[30] VDD_2V85_EMMC



[4,5,8,9,10,11,12,13,14,17,19,20,21,22,24,25,26,27,30,31,32,33]

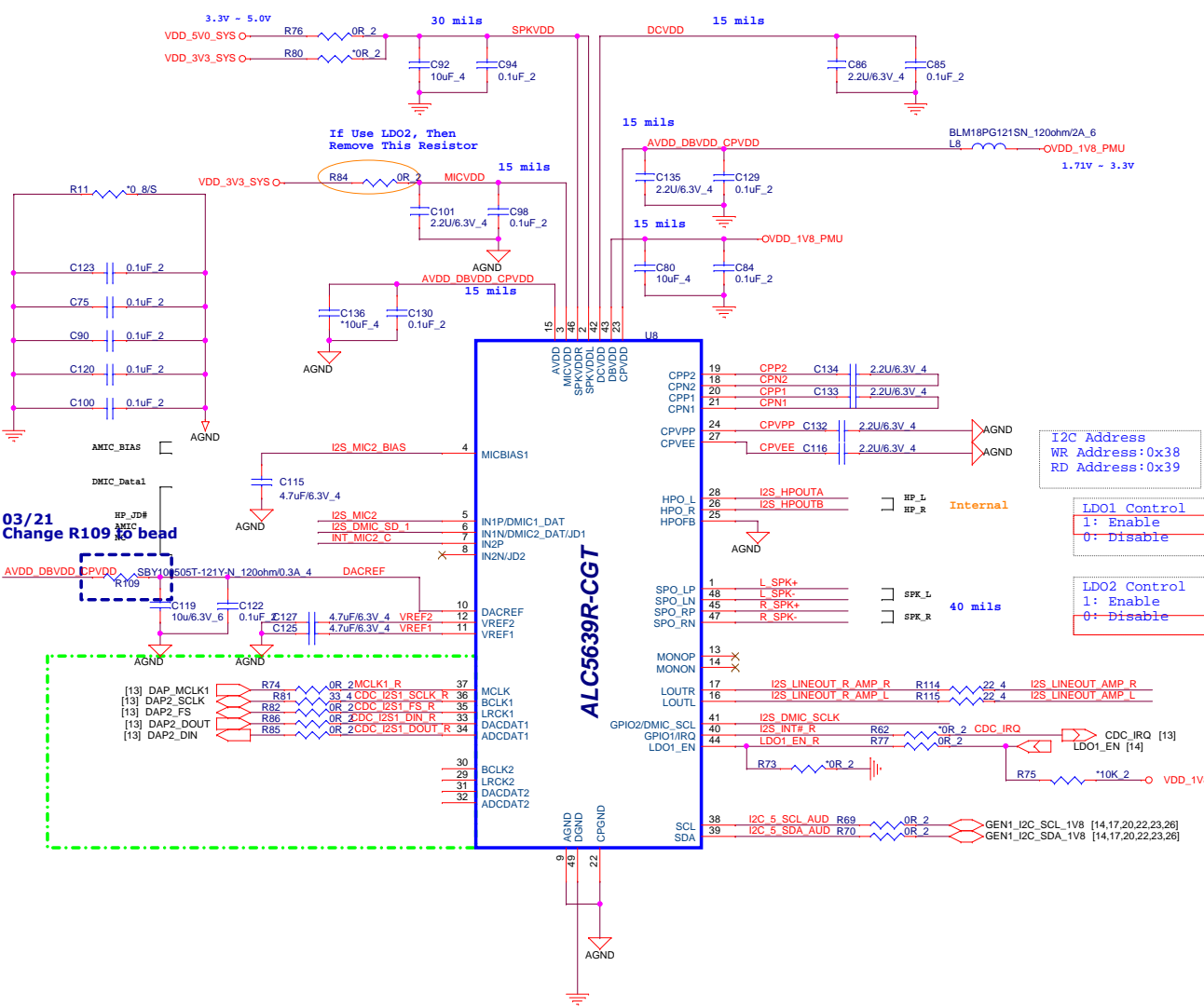
VDD_1V8_PMU



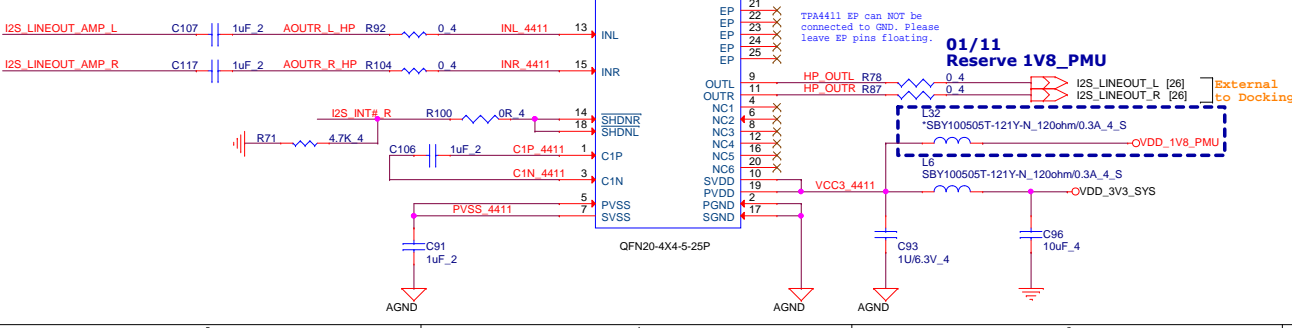
PROJECT : W02
Quanta Computer Inc.

Size	Document Number	Rev
Custom	eMMC	1A
Date: Thursday, April 18, 2013 Sheet 18 of 33		

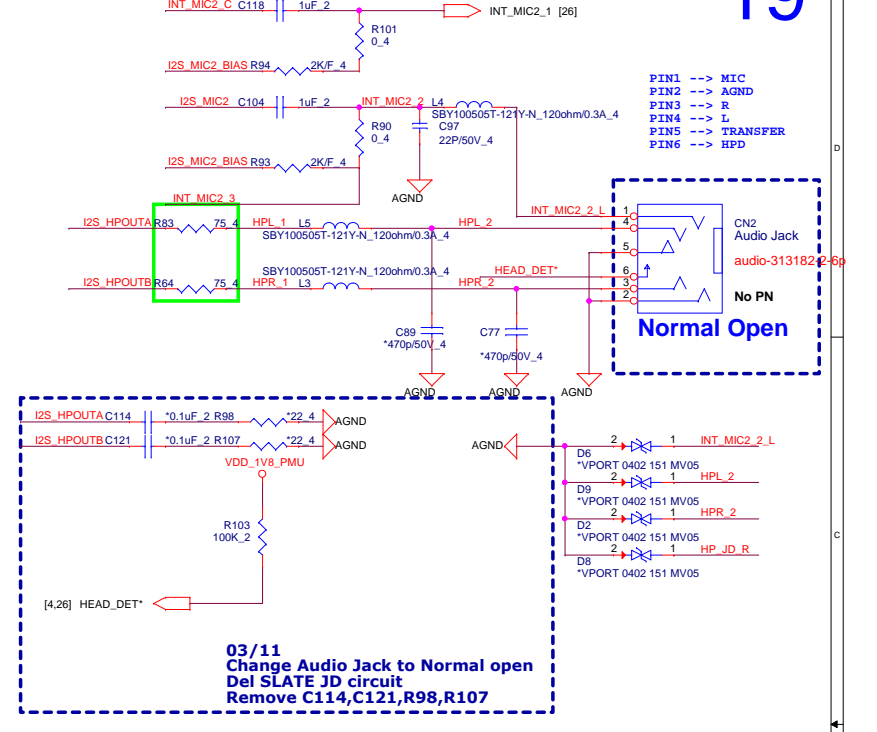
Audio Codec (ALC5640)



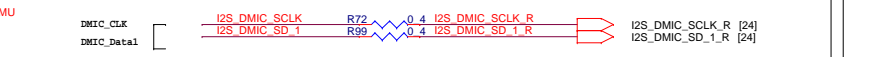
AMP to Docking



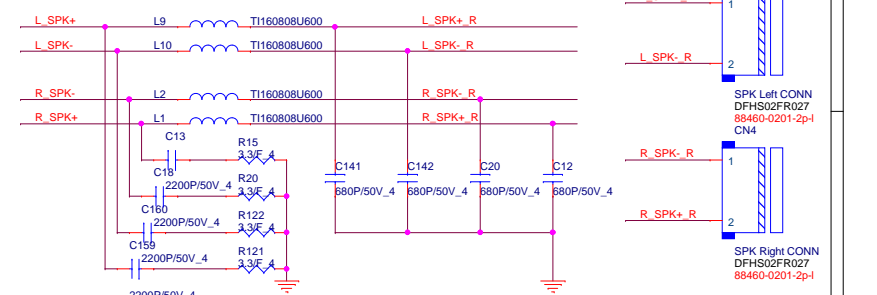
Headphone and Mic Jack

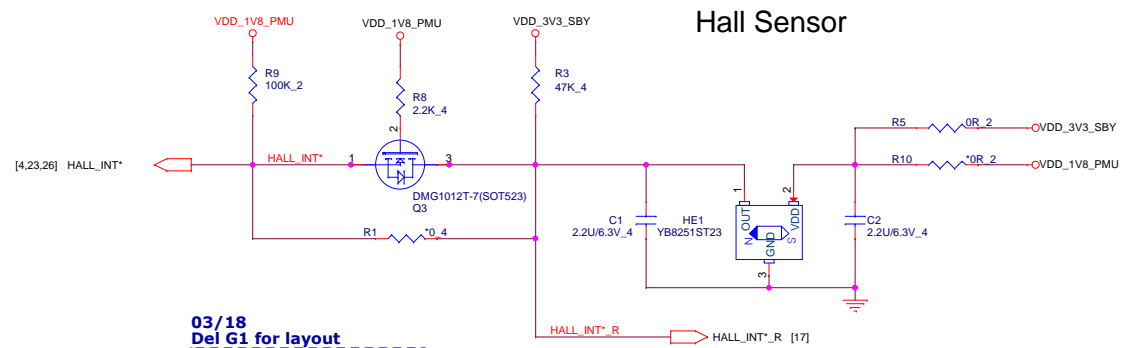
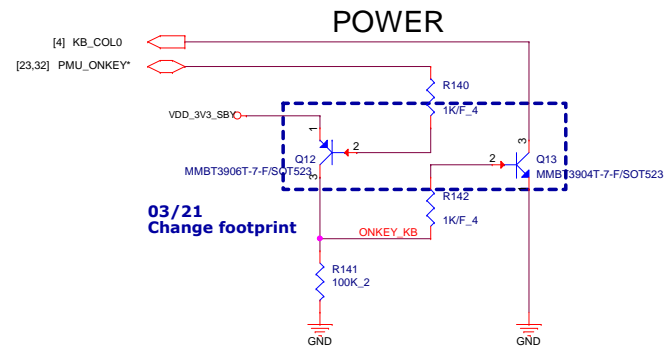
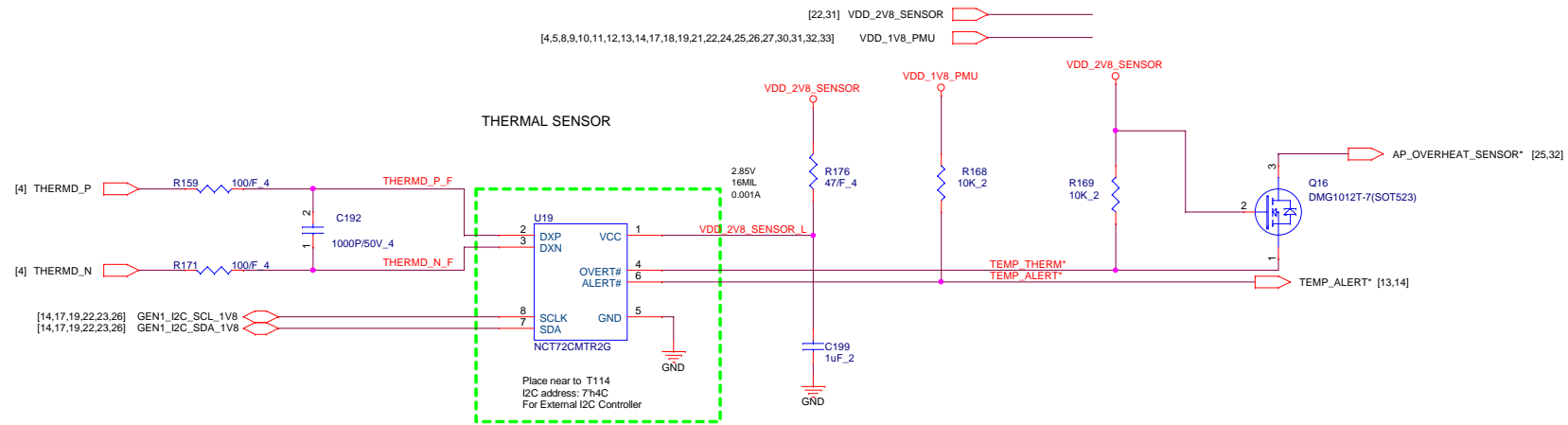


Digital MIC

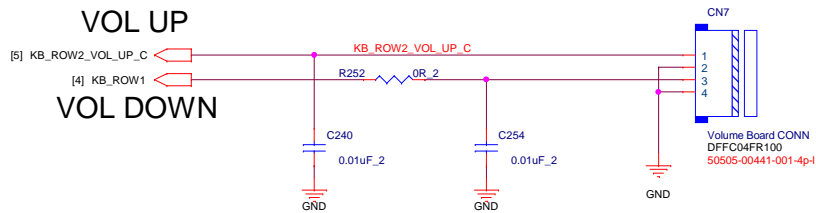
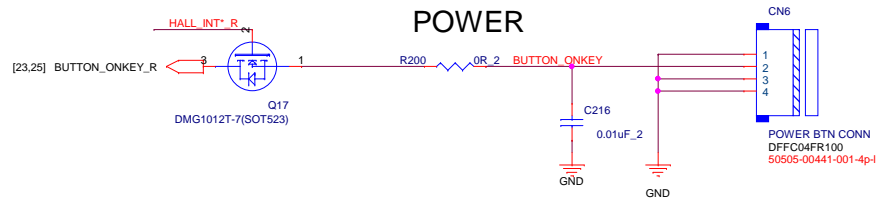
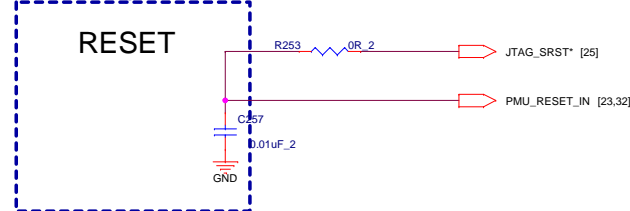


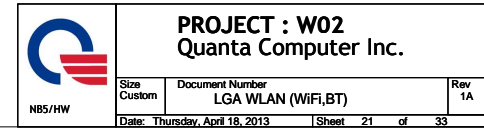
SPK trace width Speaker 4 ohm: 40mils Close to CODEC

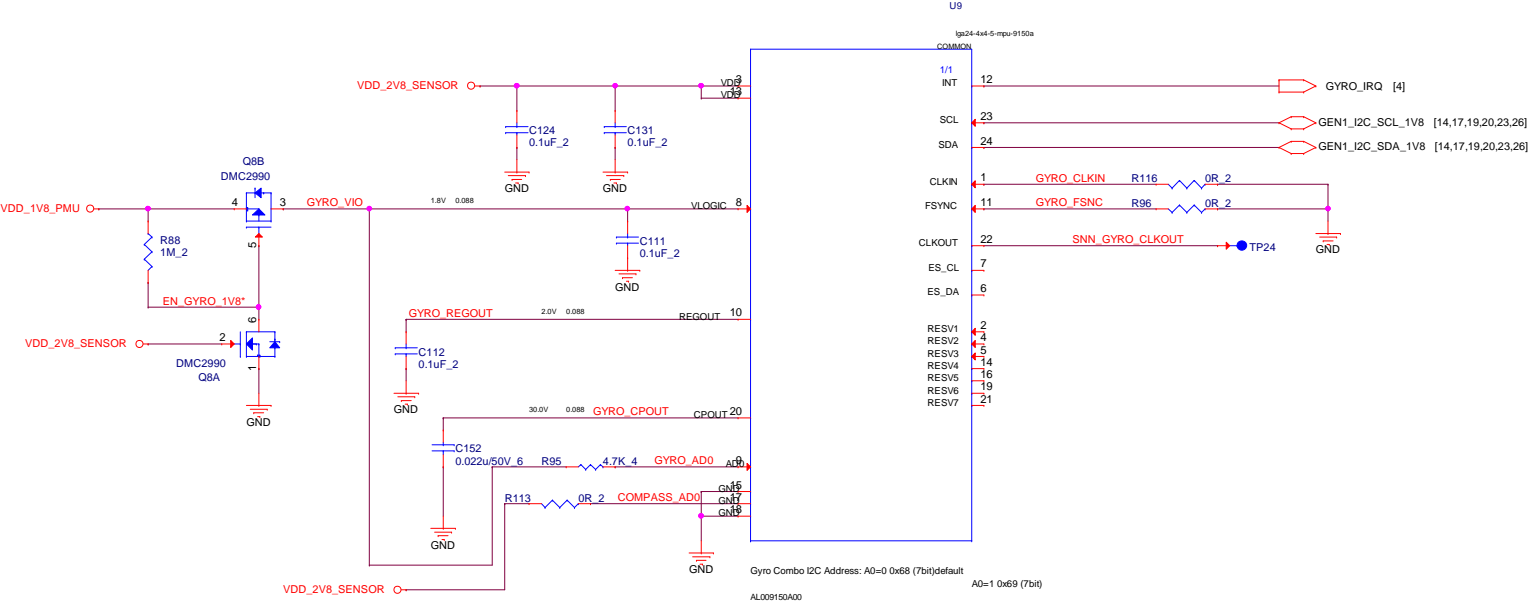




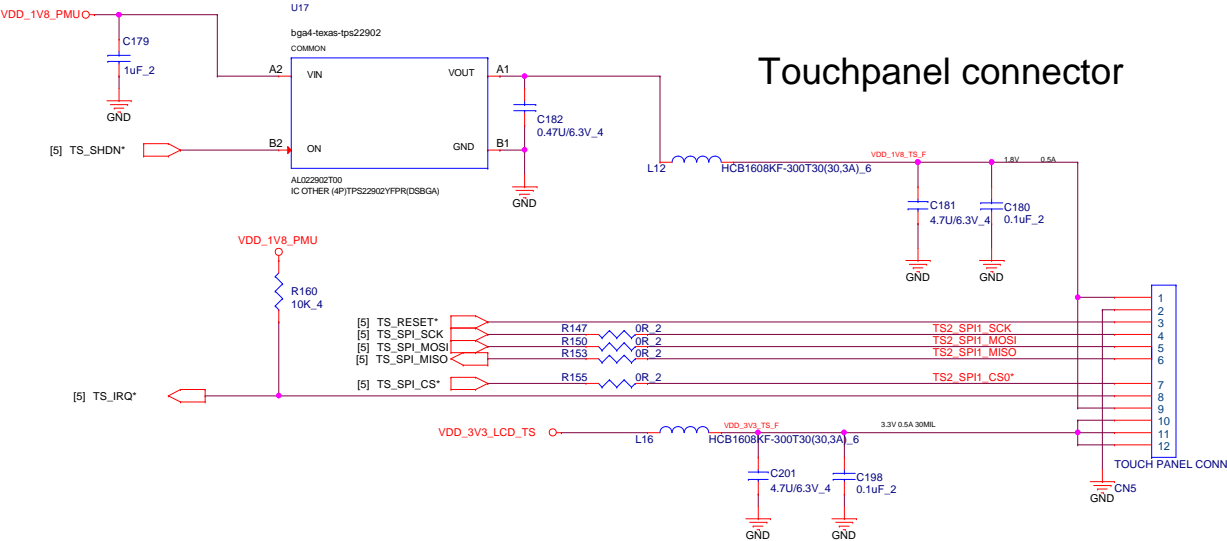
**03/18
Del G1 for layout**

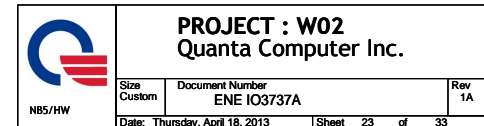






Touchpanel connector

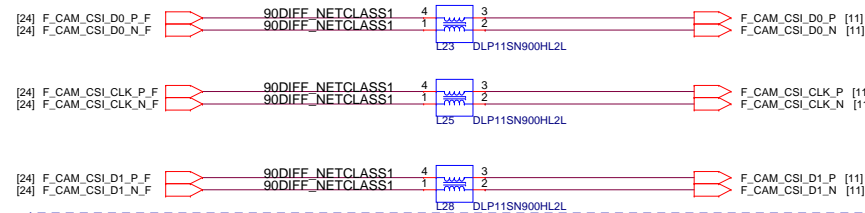




Front Camera Module Connector

Camera module connector

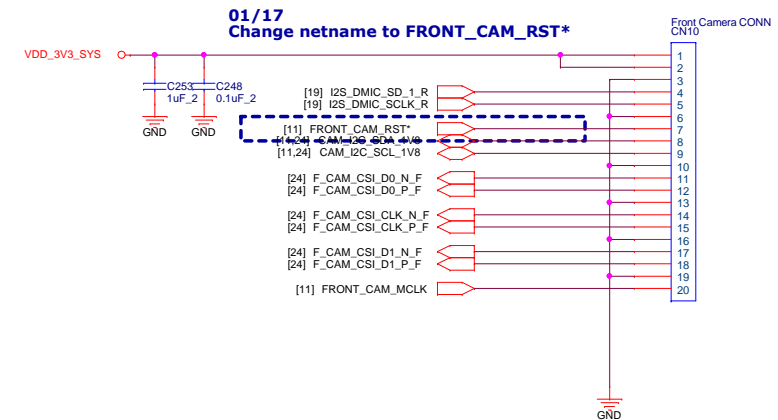
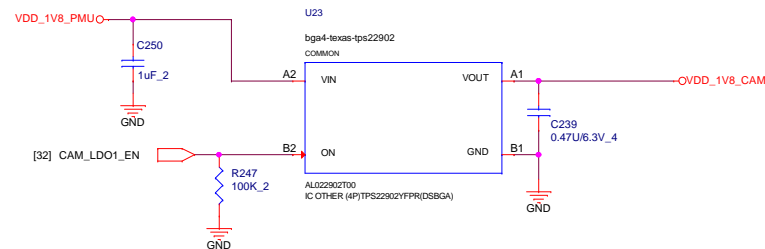
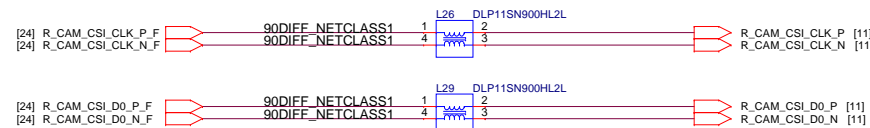
EMI/ESD



CAM_RST* Level Shifter

01/17

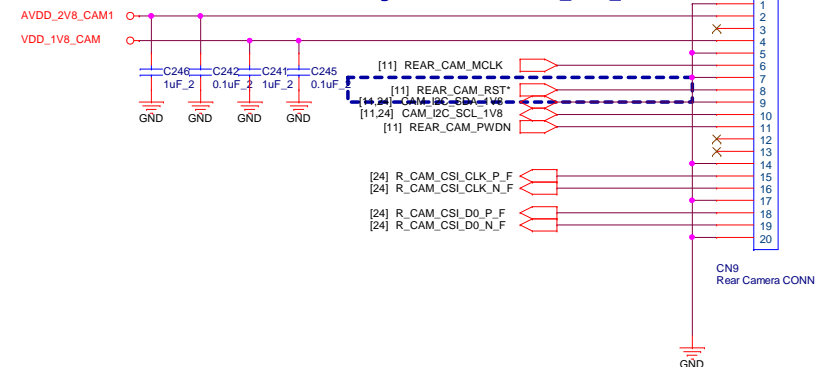
Del CAM_RST* Level Shifter



Rear Facing Camera Connector

01/17

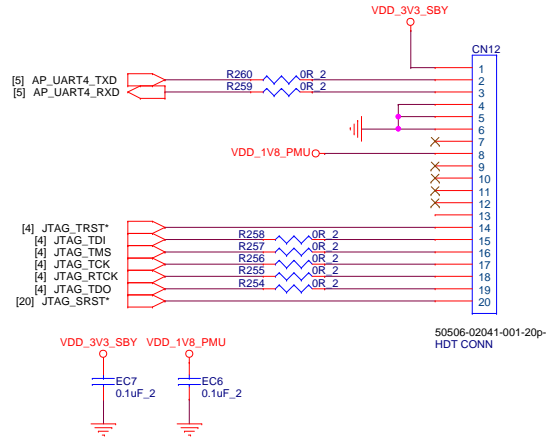
Change netname to REAR_CAM_RST*



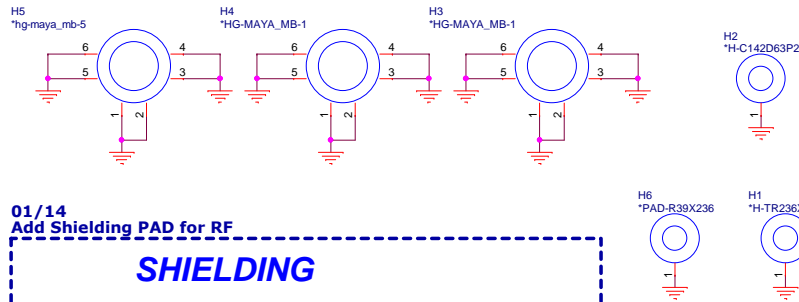
PROJECT : W02
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CAMERA	1A
Date:	Thursday, April 18, 2013	Sheet 24 of 33

MB to JTAG/UART BOARD

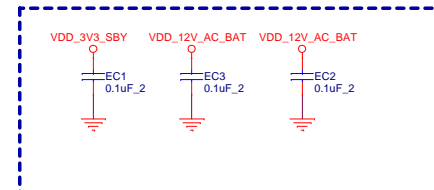
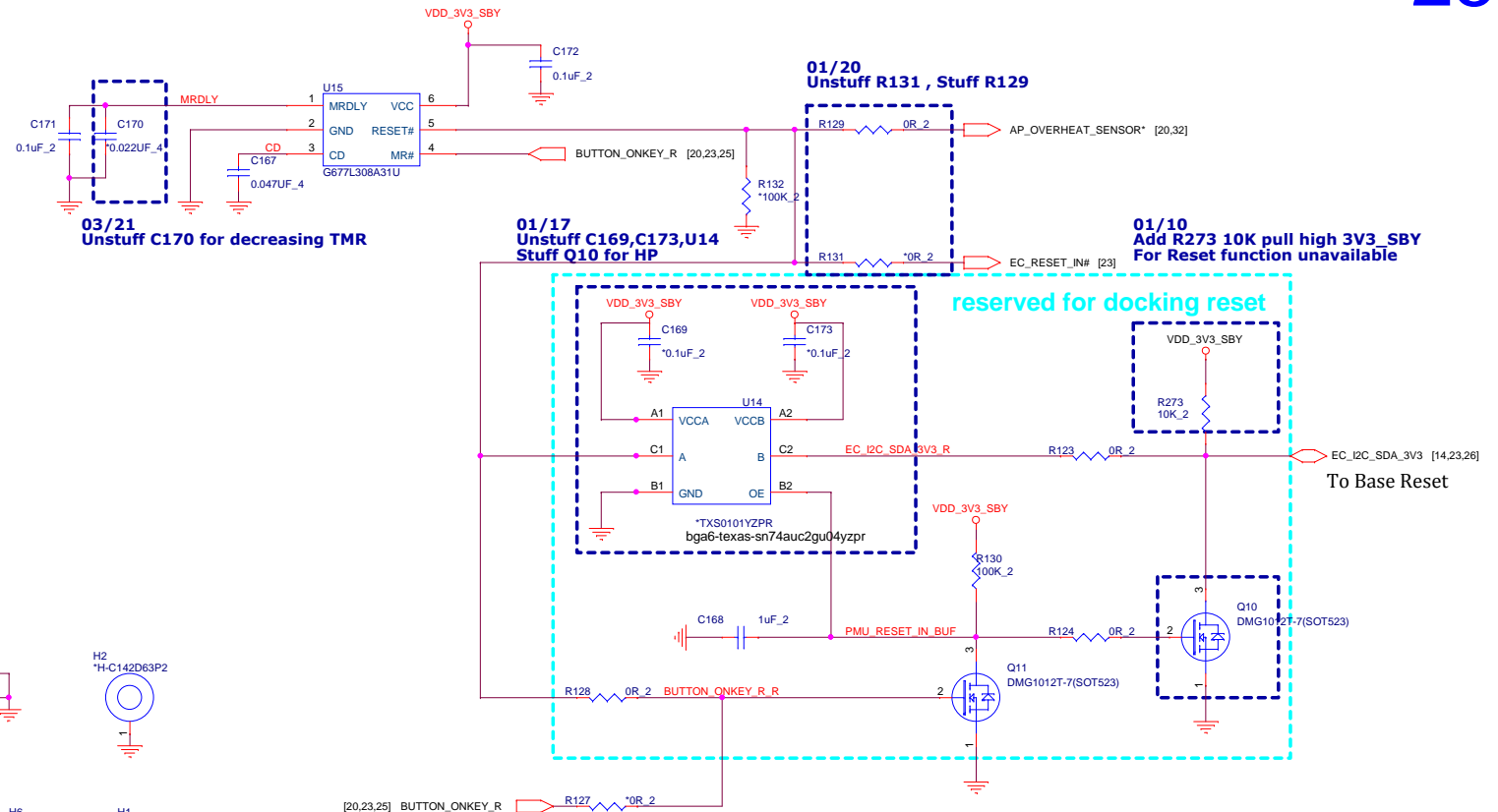
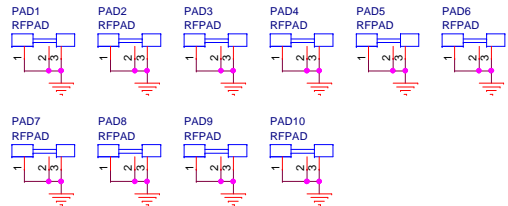


Slate Hole

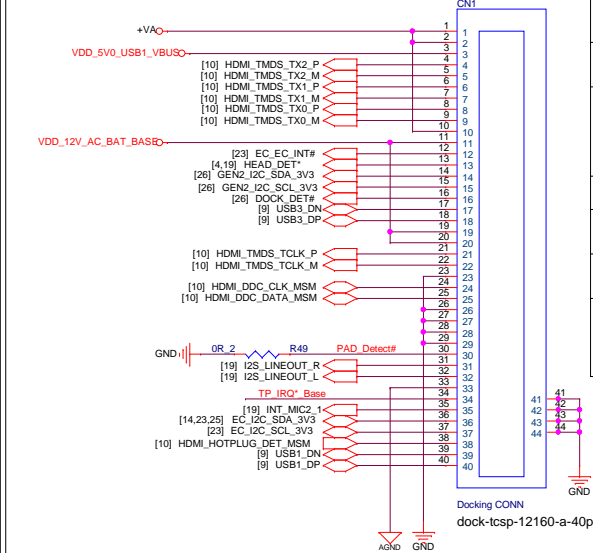


01/14 Add Shielding PAD for RF

SHIELDING

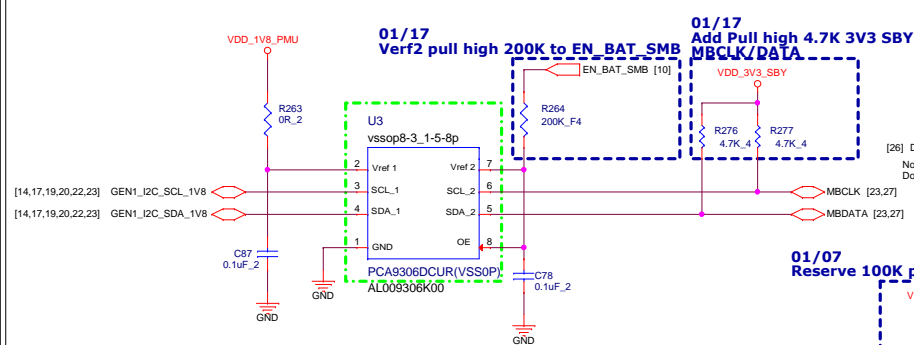


Main board to Dock board connection,

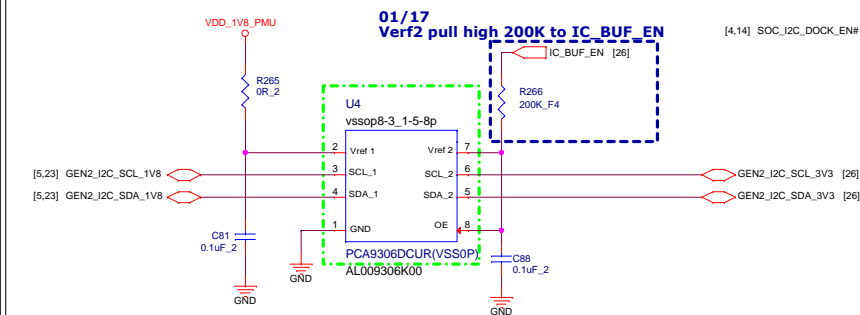


STATUS	CPU_LED_WHITE	CPU_LED_AMBER
CHARGING	L	H
NOT CHARGING	H	L
DOCKING IN or NO AC	L	L
STATUS	EC_LED_WHITE	EC_LED_AMBER
CHARGING	H	L
NOT CHARGING	L	H
DOCKING IN or NO AC	H	H

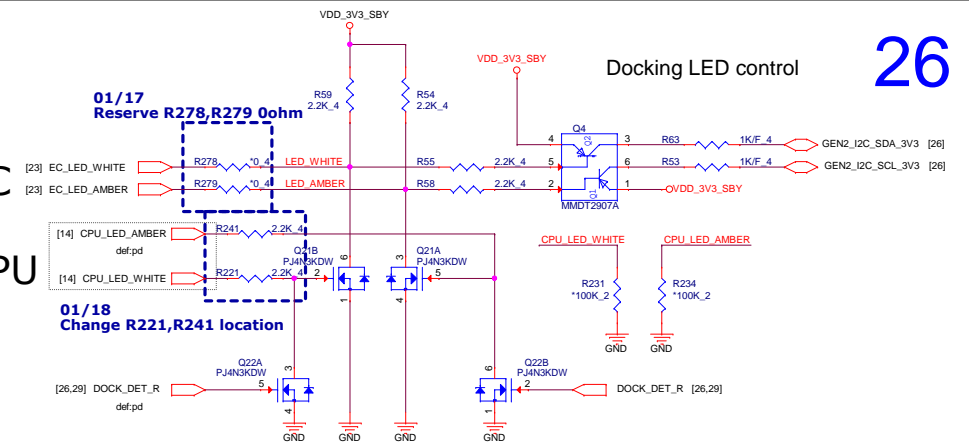
PAD_Detect# -->Base Default PU
SOC_DOCK_DET# -->Int PU (1.8V)



DOCK_DET Circuit

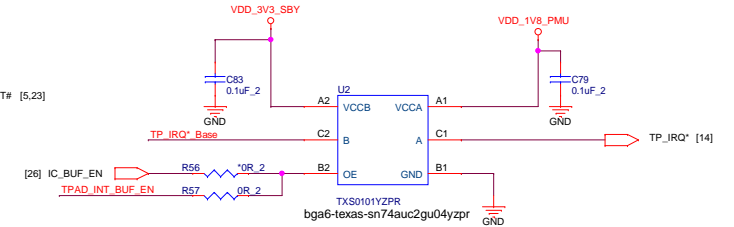


EC
CPU

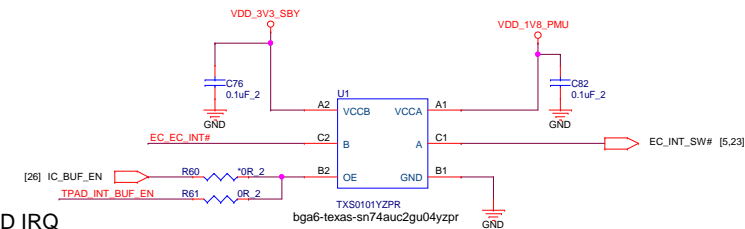


Docking LED control

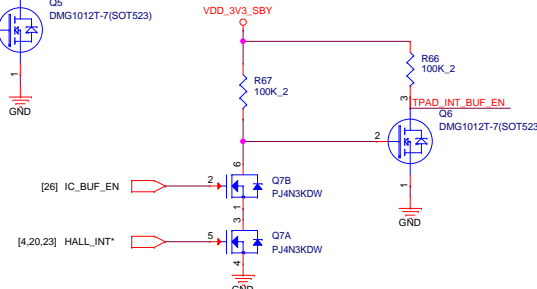
Touch PAD IRQ Level Shifter



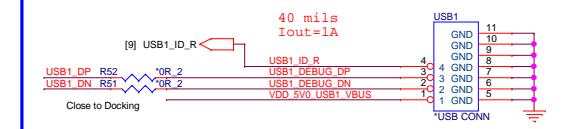
KBC IRQ Level Shifter

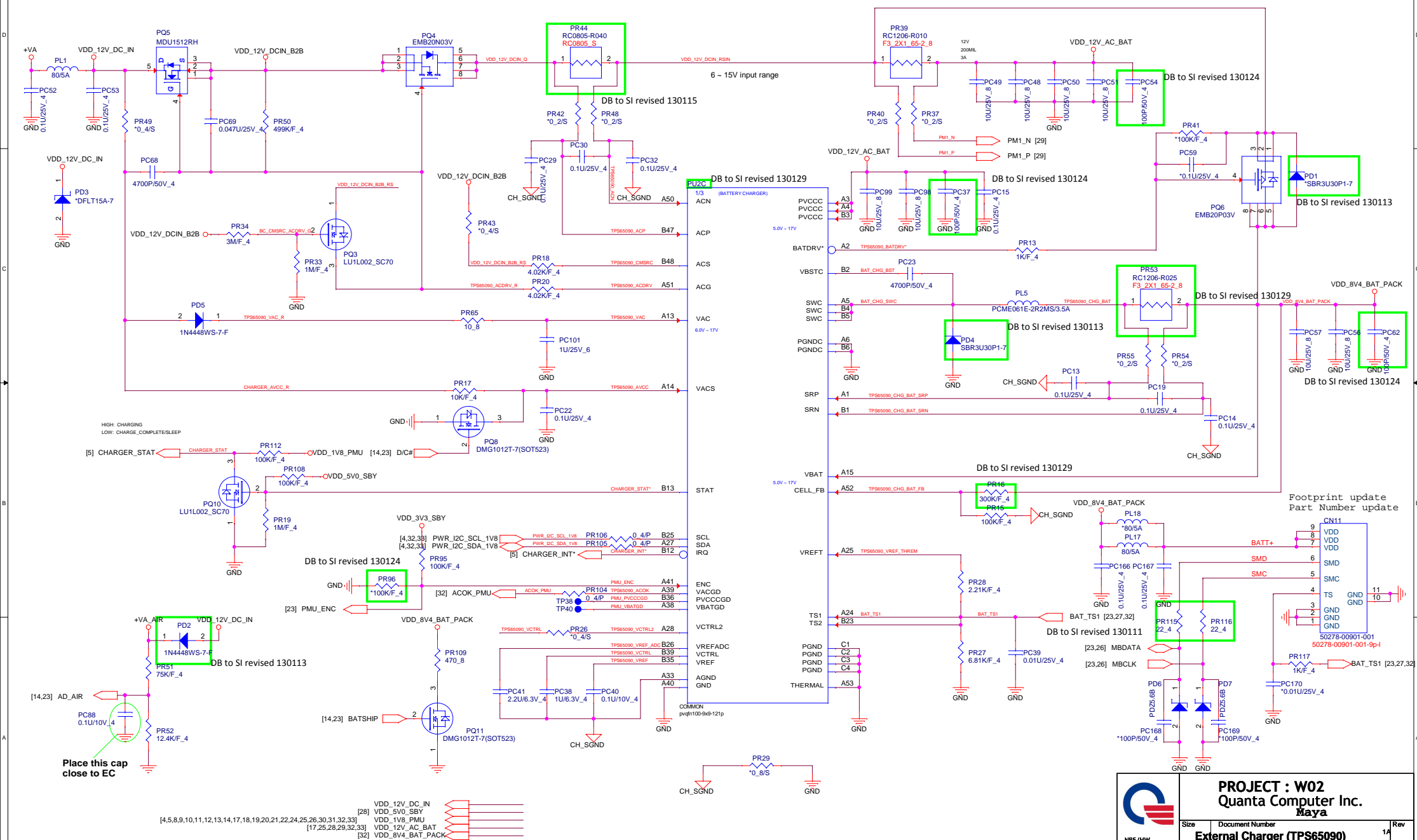


AND Logic for Touch PAD IRQ

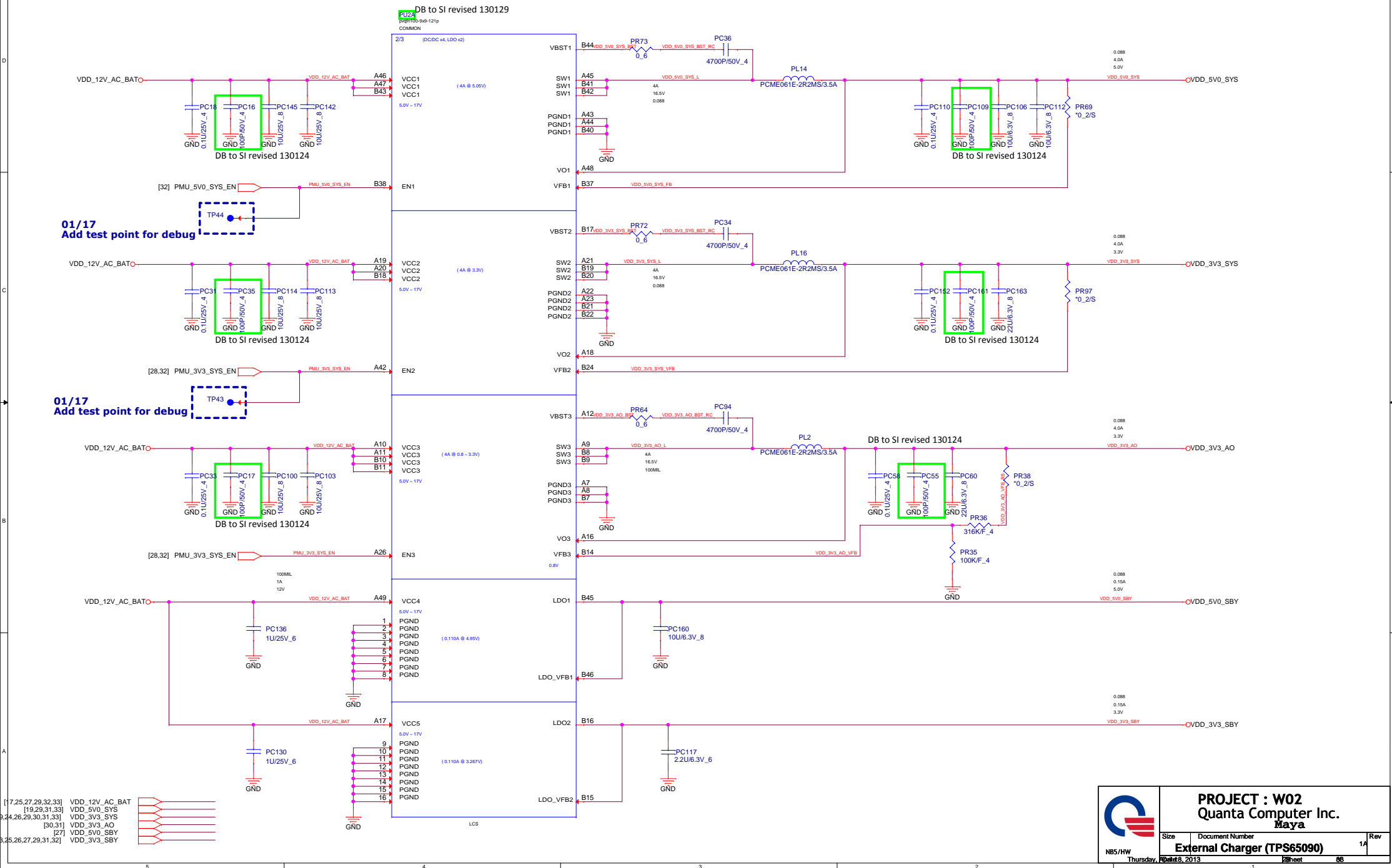


For Nvidia debug reserve

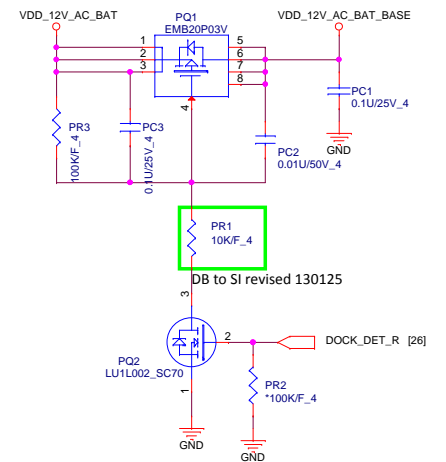
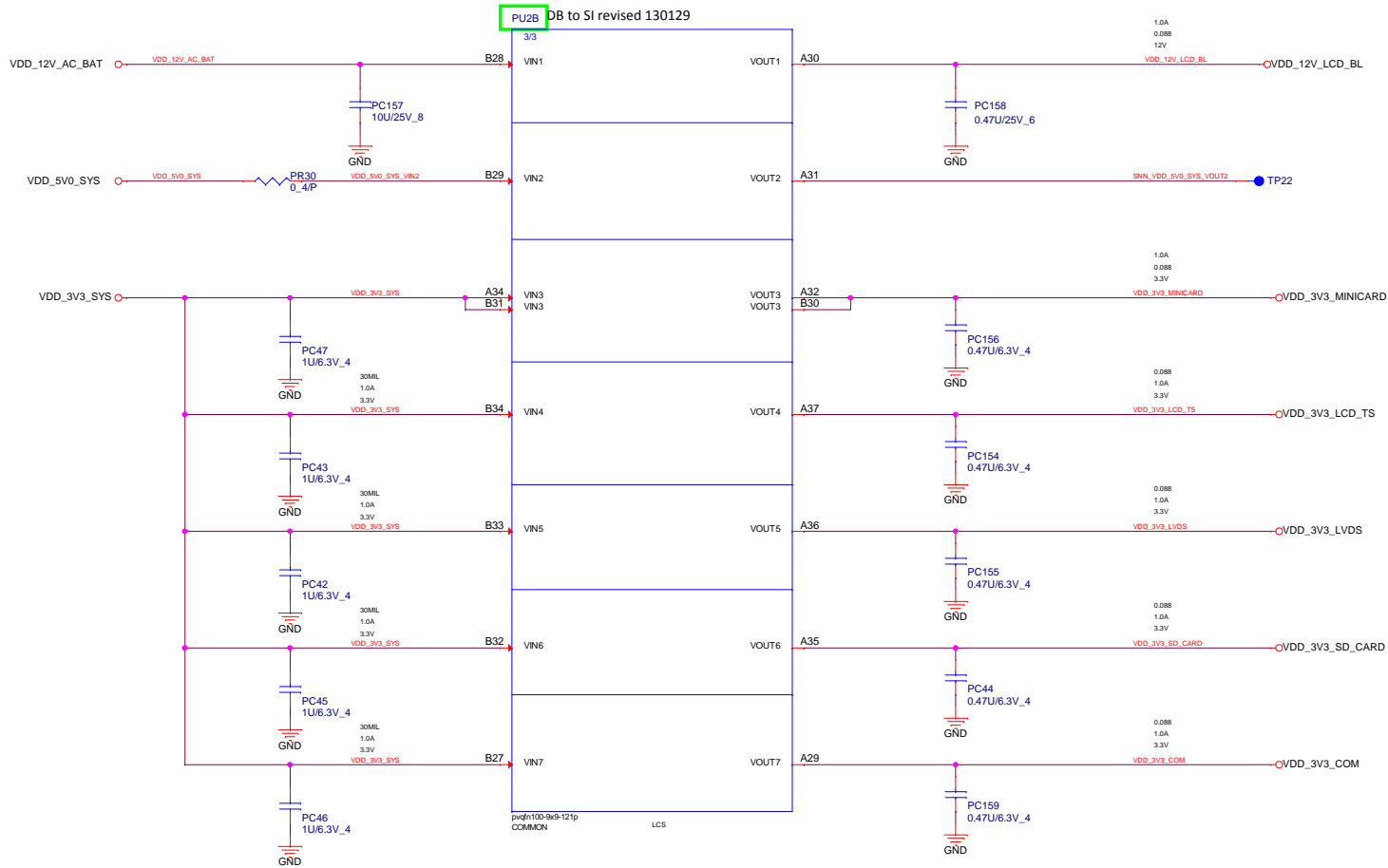




28

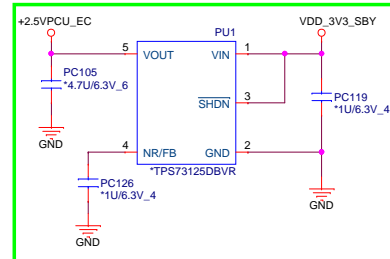


LOAD SWITCHES TPS65090 3/3

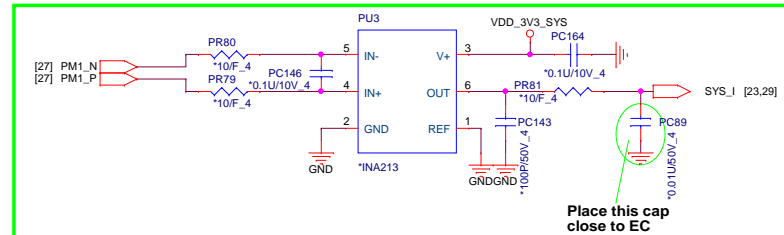


[20,23,25,26,27,28,31,32]	[23,29] SYS_I
[23]	VDD_3V3_SBY
[17,25,27,28,32,33]	+2.5VPCU_EC
[19,28,31,33]	VDD_12V_AC_BAT
[10,19,24,26,28,30,31,33]	VDD_5V0_SYS
[17]	VDD_12V_LCD_BL
[22]	VDD_3V3_MINICARD
[17]	VDD_3V3_LCD_TS
[12]	VDD_3V3_LVDS
[21]	VDD_3V3_SD_CARD
[21]	VDD_3V3_COM

DB to SI revised 130124

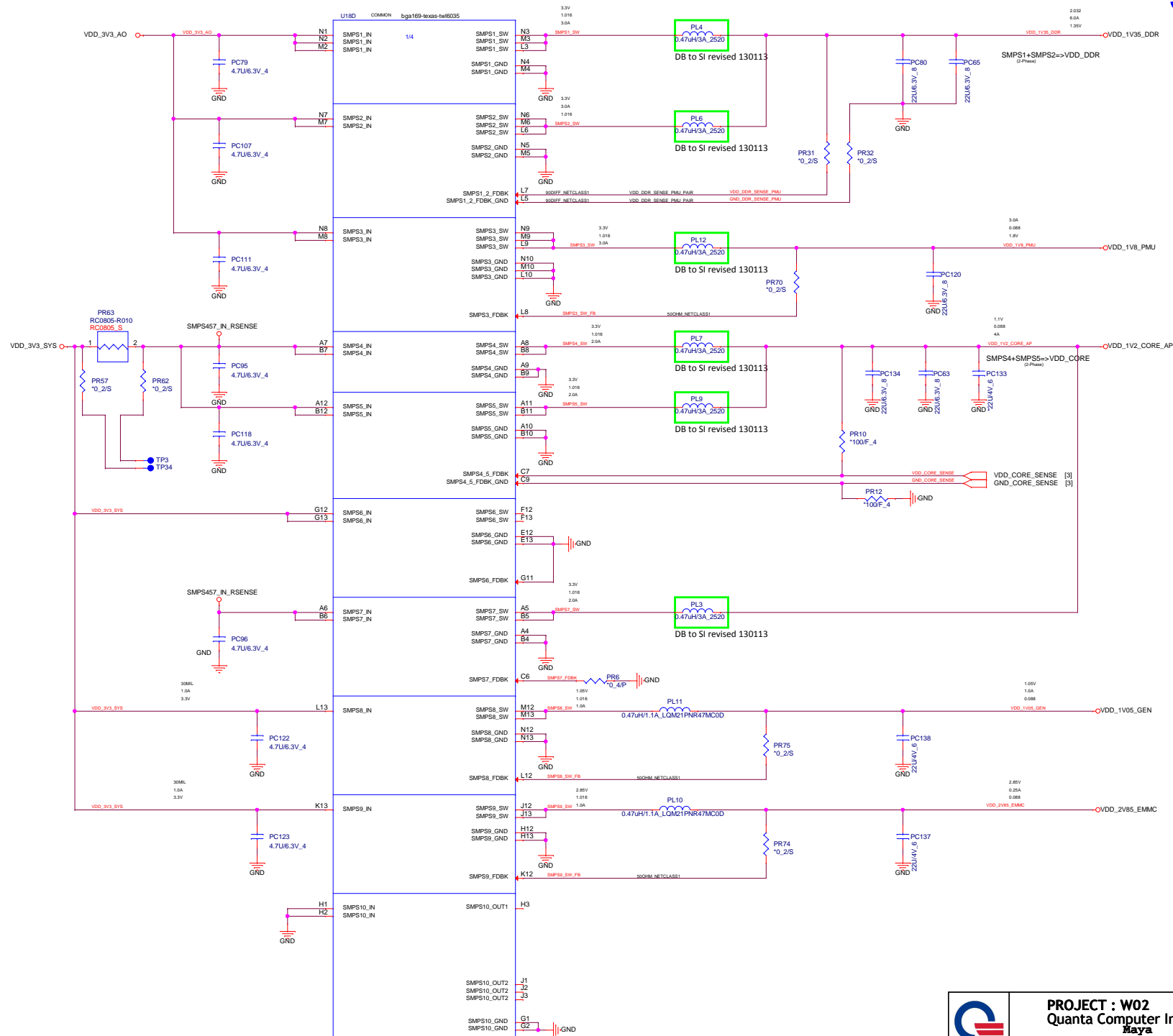


DB to SI revised 130125



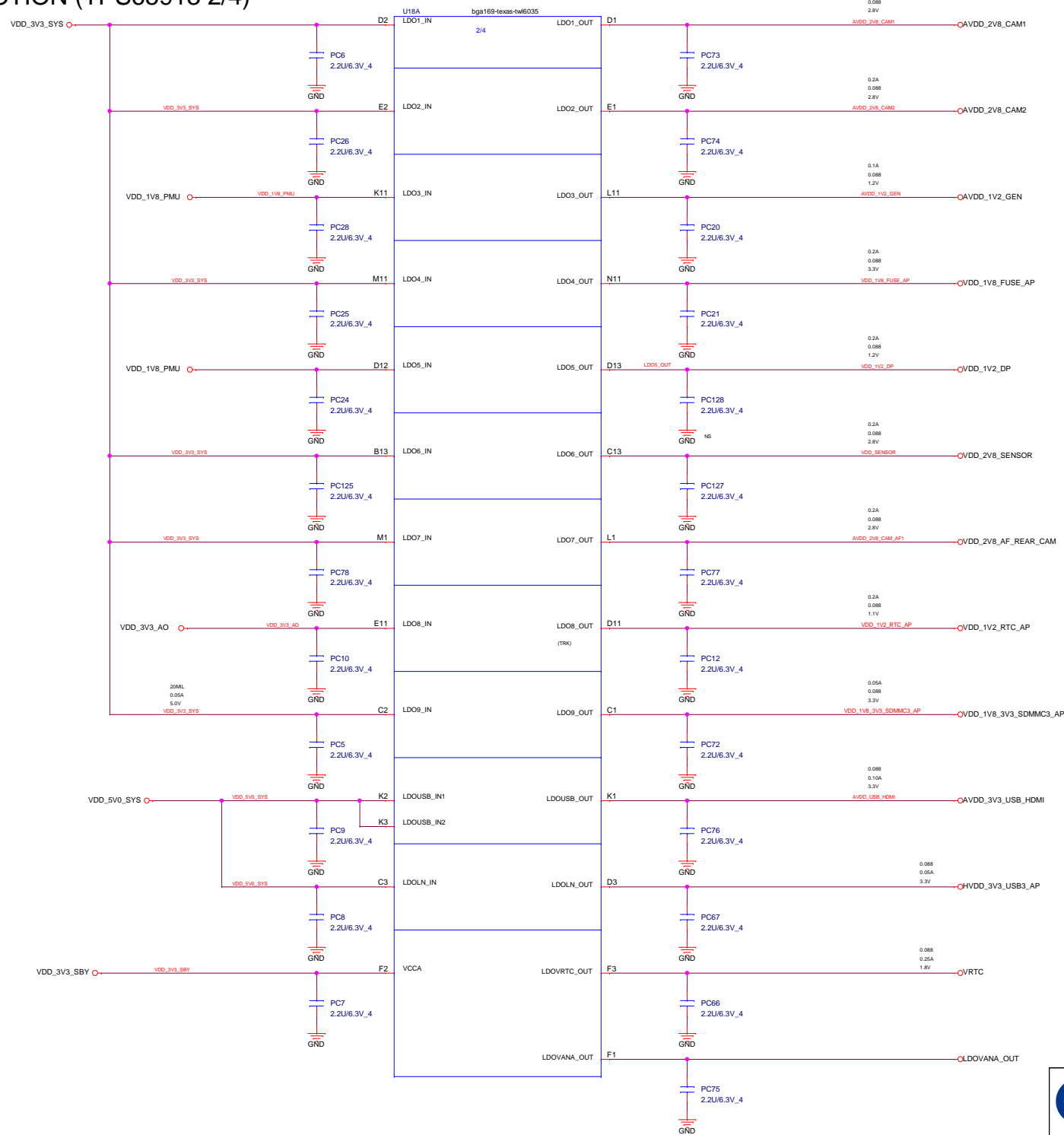
PMU SWITCHING REGULATOR SECTION (TPS65913 1/4)	
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30



PMU LDOs SECTION (TPS65913 2/4)

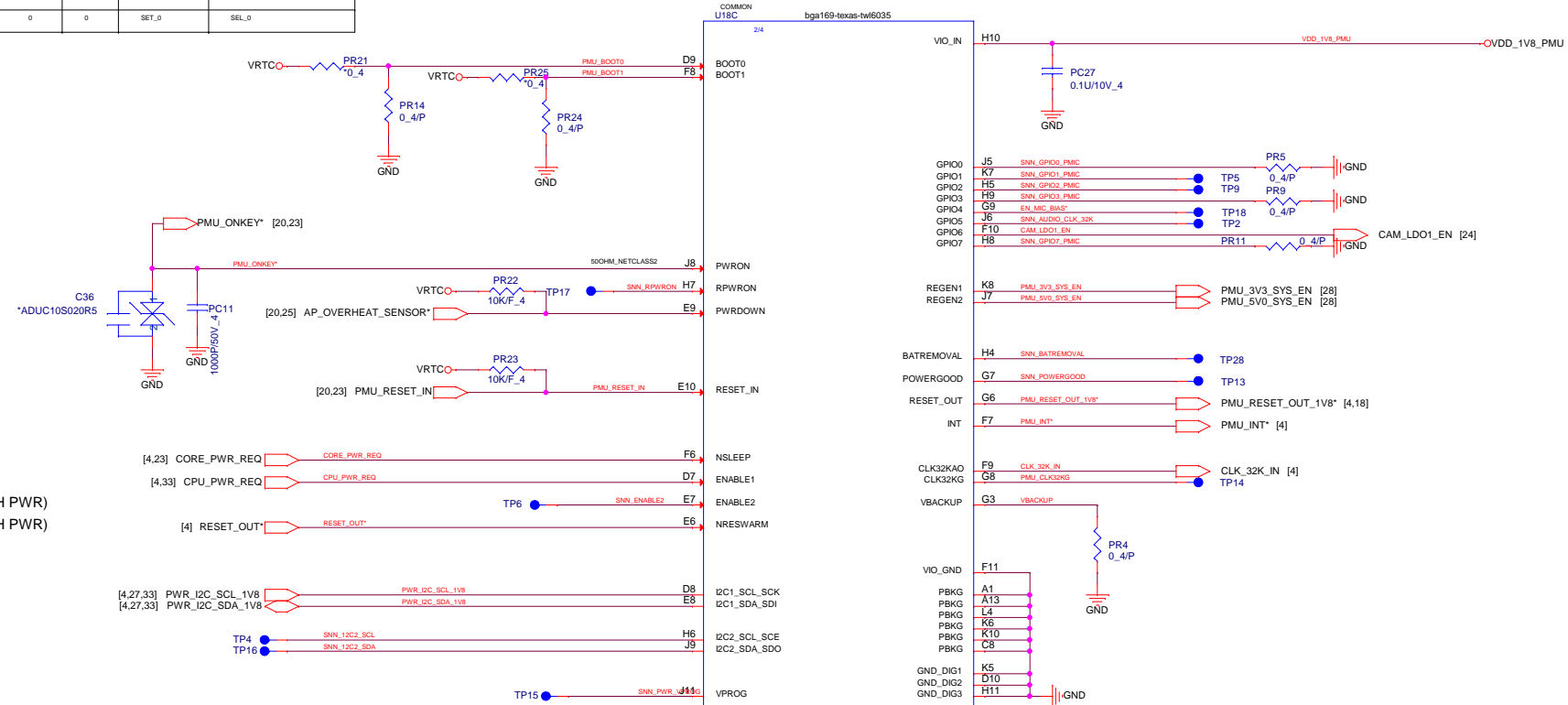
31



PMU LOGIC SECTION (TPS65913 3/4)& ANALOG SECTION(TPS65913 4/4)

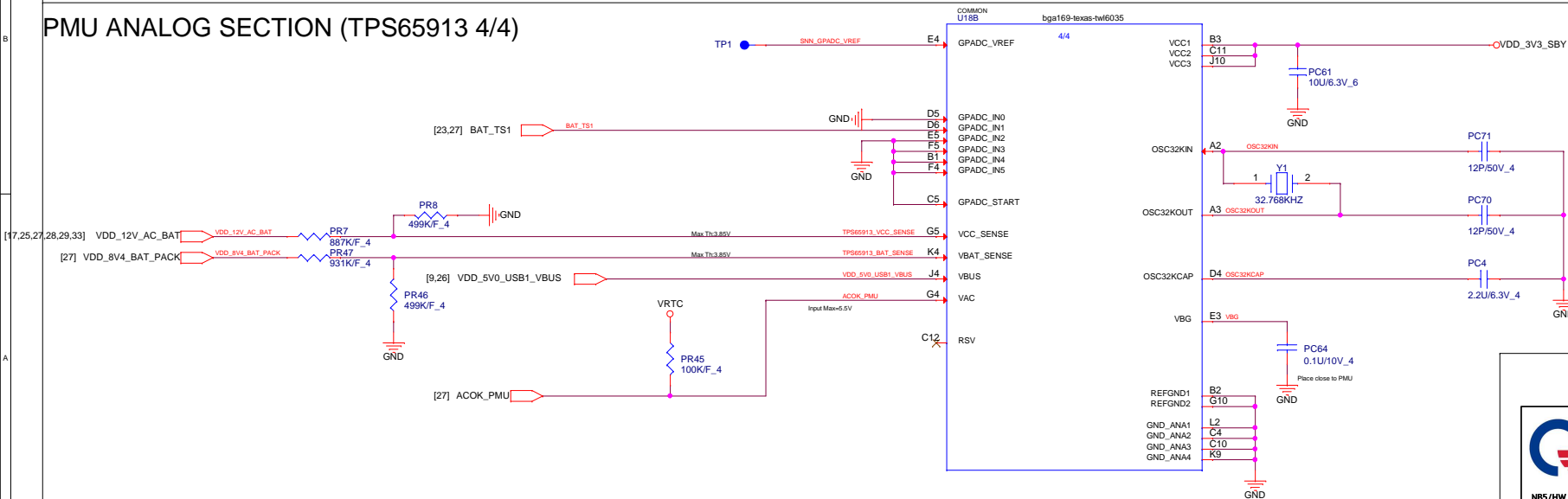
PMU LOGIC SECTION (TPS65913 3/4)

BOOT0	BOOT1	OTP_CONFIG	POWER_SEQ_SELECTOR
0	0	SET_0	SEL_0



1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

PMU ANALOG SECTION (TPS65913 4/4)





Size	Document Number
	CPU_CORE (TPS51622RSML)